Design and Analysis of Cascode Amplifier Using g_m/I_D and PDM Methodologies

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***Abstract*—Cascode amplifiers are widely used in high-gain and high-bandwidth analog circuit applications due to their superior output resistance and reduced Miller capacitance. This work presents the complete design methodology, small-signal analysis, pole-zero analysis, and Cadence simulation verification of cascode amplifiers using both resistive load and current-source load techniques. The g_m/I_D methodology and PDM-based design approaches are implemented to obtain optimized transistor sizing, biasing conditions, and frequency response characteristics. The results demonstrate the effectiveness of cascode architecture in achieving high gain, improved stability margins, and extended bandwidth suitable for modern CMOS analog systems.**

I. Introduction

Modern analog integrated circuits require amplifiers that provide high gain while maintaining large bandwidth and good stability margins. The cascode amplifier is one of the most important topologies used to achieve these requirements because it increases output resistance and suppresses the Miller multiplication effect.

The architecture combines a common-source transistor with a common-gate transistor, which effectively isolates the input node from output voltage variations. This isolation leads to reduced parasitic capacitance interaction and improved frequency performance.

Applications of cascode amplifiers include:

- Operational amplifiers
- RF front-end amplifiers
- Analog signal conditioning blocks
- High-speed data converters

The design in this work is performed using Cadence Virtuoso and validated through DC, AC, transient, and pole-zero simulations.

II. Cascode Amplifier Fundamentals

A. Circuit Operation

The cascode amplifier consists of two MOSFET devices:

- M_1 — input common-source transistor
- M_2 — common-gate transistor providing high output resistance

Figure 1 shows the cascode configuration used for analysis.

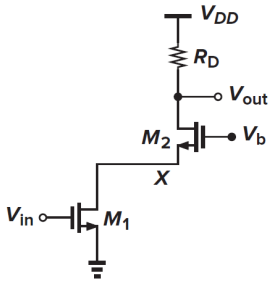

Fig. 1: Basic cascode amplifier configuration

B. Image Analysis

The schematic illustrates the biasing arrangement where the drain of the input transistor connects to the source of the cascode transistor. This node, often called the internal high-impedance node, is shielded from output voltage variations by the common-gate transistor. Such shielding reduces the effective capacitance seen at the input transistor, enabling higher bandwidth operation compared to simple common-source amplifiers.

Furthermore, the load resistor connected at the output converts the output current into voltage, establishing the overall gain mechanism.

III. Small Signal Analysis

In the ideal case, assuming infinite output resistance, the small-signal drain current produced by the input transistor is

$$i_d = g_{m1} v_{in} \tag{1}$$

The input resistance at the source of the cascode device becomes

$$r_x = \frac{1}{g_{m2} + g_{mb2}} \tag{2}$$

Because the source voltage variation is limited, the current flowing through the cascode device remains nearly constant, improving gain stability. This leads to the fundamental cascode gain expression

$$A_v = -g_{m1}(R_D \parallel R_{out}) \tag{3}$$

where the effective output resistance is greatly enhanced by transistor stacking.

IV. Output Resistance Enhancement

The major advantage of the cascode configuration is the multiplication of output resistance, given approximately by

$$R_{out} \approx g_{m2} r_{o1} r_{o2} \tag{4}$$

This shows that even moderately large transistor output resistances can produce very high overall gain when cascoded.

V. Frequency Response and Stability Considerations

Cascode amplifiers exhibit improved high-frequency performance because the Miller capacitance associated with the input transistor is minimized. As a result, the dominant pole is pushed to higher frequencies, increasing bandwidth while maintaining sufficient phase margin for stability.

VI. g_m/I_D Based Design Methodology

The g_m/I_D methodology provides a systematic approach for transistor sizing by directly relating transconductance efficiency to device bias current. Unlike traditional square-law based sizing methods, this approach enables designers to select the appropriate operating region (weak, moderate, or strong inversion) depending on performance targets such as power efficiency, speed, and gain.

For high-speed analog circuits, devices are typically biased in moderate inversion, where an optimal compromise between intrinsic gain and transit frequency is achieved.

A. Design Specifications

The design specifications used for the cascode amplifier with resistive load are summarized as follows:

- Supply voltage $V_{DD} = 1.8\,V$
- Power consumption $P = 1\,mW$
- Target gain $A_v = 20\,dB$
- Load capacitance $C_L = 5\,pF$
- Required bandwidth $f_{-3dB} = 20\,MHz$

From the power specification,

$$I_D = \frac{P}{V_{DD}} = 5.55 \times 10^{-4} A \tag{5}$$

Selecting the output DC operating point near mid-supply maximizes output swing:

$$R_D = \frac{V_{DD}}{2I_D} \approx 1.6k\Omega \tag{6}$$

Since the required gain is $10\,V/V$,

$$g_m = \frac{A_v}{R_D} = 6.25mS \tag{7}$$

Thus the transconductance efficiency becomes

$$\frac{g_m}{I_D} \approx 13.5 \tag{8}$$

This value indicates that the device is biased in the moderate inversion region, which is desirable for high-gain low-power operation.

VII. Device Sizing Using Lookup Curves

A. Bottom NMOS Sizing

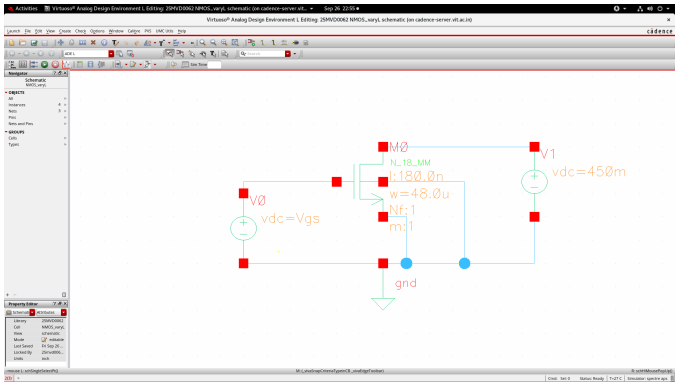

Fig. 2: Testbench setup used to generate g_m/I_D characteristics

Image interpretation: The above schematic shows the characterization setup used in Cadence to extract transistor performance parameters. By sweeping gate voltage while maintaining constant drain current density, lookup curves for g_m/I_D and I_D/W are generated. These curves serve as technology-specific design references that eliminate the need for analytical transistor models during sizing.

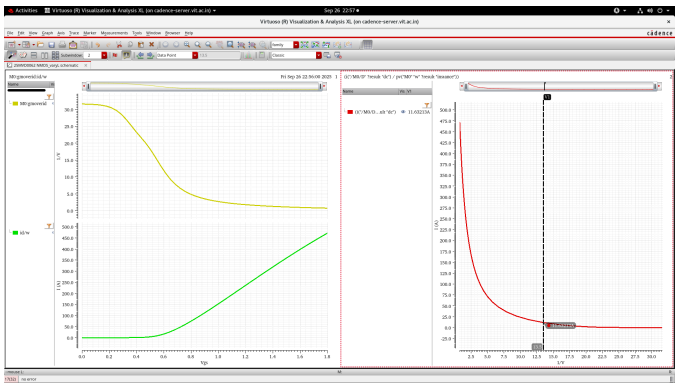

Fig. 3: I_D/W versus g_m/I_D characteristic

Image interpretation: This plot represents the trade-off between current density and transconductance efficiency. Higher g_m/I_D corresponds to weak inversion operation with higher gain efficiency but lower speed, whereas smaller values correspond to strong inversion with higher speed but lower intrinsic gain. Selecting $g_m/I_D = 13.5$ ensures that the transistor operates in moderate inversion, balancing gain and bandwidth.

From the graph,

$$\frac{I_D}{W} = 11.63 \tag{9}$$

Hence,

$$W = \frac{I_D}{I_D/W} = 48\mu m \tag{10}$$

B. Gate Bias Determination

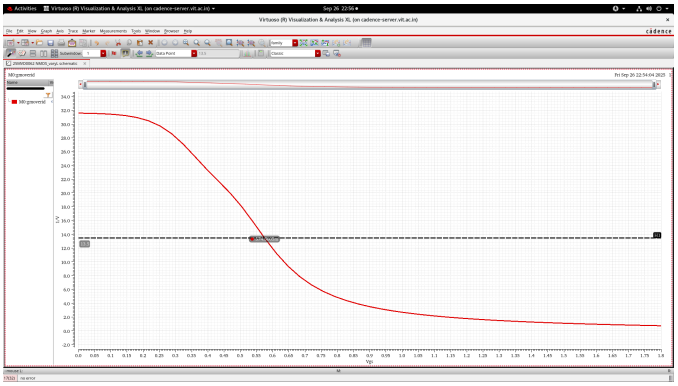

Fig. 4: g_m/I_D versus V_{GS} characteristic

Image interpretation: This curve shows the relationship between gate voltage and transconductance efficiency. The region where the curve begins to flatten indicates strong inversion, while the steep portion corresponds to weak inversion. The selected operating point at $g_m/I_D = 13.5$ corresponds to approximately $V_{GS} = 0.574V$, ensuring moderate inversion biasing.

VIII. Top NMOS Device Sizing

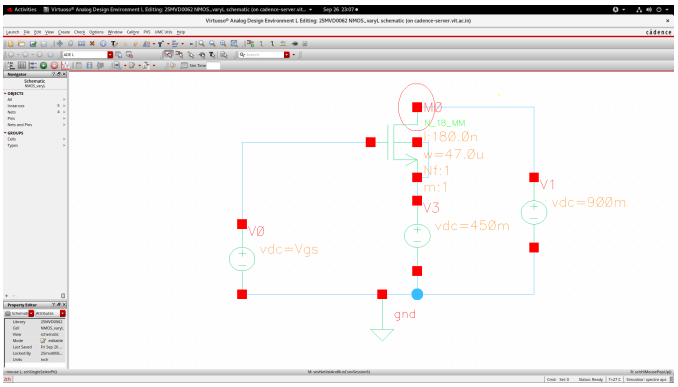

Fig. 5: Cascode device characterization setup

Image interpretation: This schematic characterizes the cascode transistor separately to determine its optimum biasing conditions. Since the cascode device mainly enhances output resistance rather than transconductance, it is sized to maintain sufficient overdrive voltage while keeping parasitic capacitances minimal.

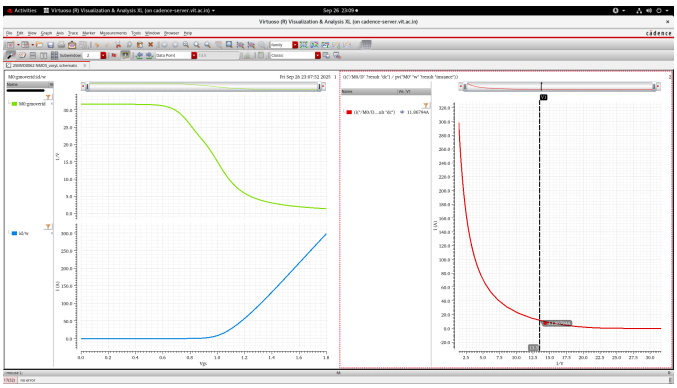

Fig. 6: I_D/W versus g_m/I_D for cascode device

From the lookup curve,

$$W_2 \approx 47\mu m \tag{11}$$

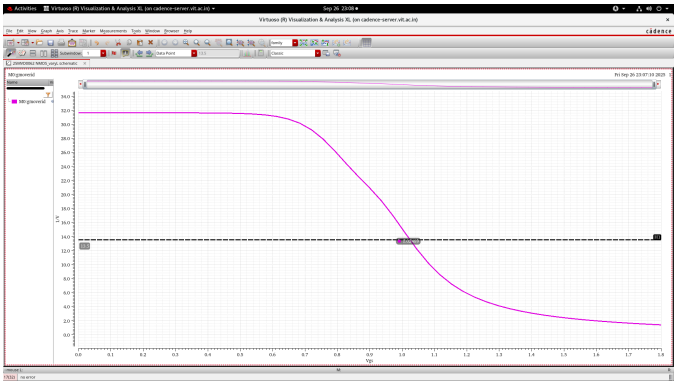

Fig. 7: g_m/I_D versus V_{GS} for cascode device

Image interpretation: The larger gate voltage required for the cascode transistor reflects its higher bias node voltage. Maintaining proper biasing ensures that both transistors remain in saturation across the full output swing, preventing gain degradation.

IX. Bias Voltage Selection

The cascode gate voltage is selected using

$$V_G = V_{GS} + V_S \tag{12}$$

ensuring that the lower transistor remains in saturation for the entire input range. Proper bias selection is essential because incorrect biasing can push the device into triode operation, reducing amplifier gain and linearity.

X. Complete Amplifier Implementation

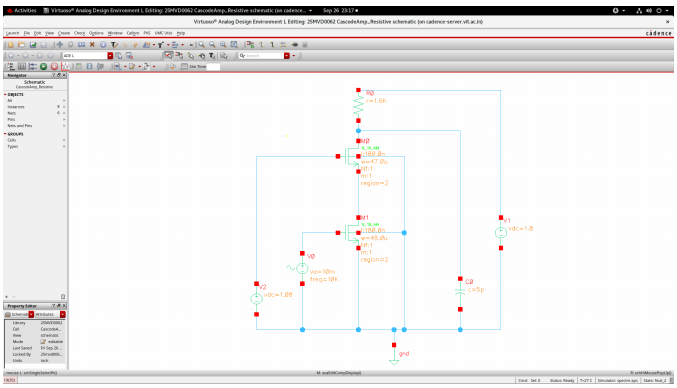

Fig. 8: Complete cascode amplifier schematic

Image interpretation: The final schematic integrates both NMOS devices, bias network, and load resistor to realize the full amplifier. The bias voltages stabilize the operating points while ensuring sufficient headroom for signal swing. Device dimensions obtained from the g_m/I_D methodology provide the required gain and bandwidth performance simultaneously.

XI. AC Response Analysis

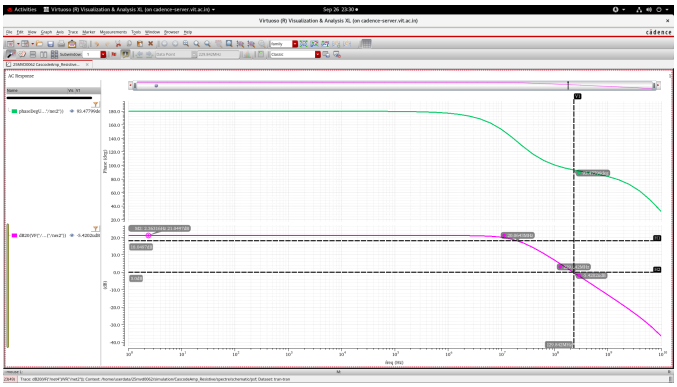

Fig. 9: AC gain response of cascode amplifier with resistive load

A. Gain Characteristics

The AC response plot shown in Fig. 9 illustrates the magnitude and phase behavior of the cascode amplifier across frequency. In the low-frequency region, the amplifier exhibits a constant midband gain of approximately 21 dB, which closely matches the theoretical design target of 20 dB derived from the small-signal gain expression. The flat region indicates that the amplifier operates in the region where capacitive effects are negligible and gain is determined primarily by transistor transconductance and load resistance.

As frequency increases, the gain begins to roll off due to the presence of parasitic capacitances associated with MOSFET gate-drain overlap, junction capacitances, and load capacitance. The frequency at which the gain decreases by 3 dB from its midband value defines the amplifier bandwidth.

B. Bandwidth Determination

The observed cutoff frequency is approximately $20\,MHz$, confirming that the transistor sizing obtained using the g_m/I_D methodology successfully satisfies the design specifications. The high bandwidth achieved demonstrates the effectiveness of the cascode configuration in suppressing the Miller multiplication effect, which otherwise limits the speed of common-source amplifiers.

XII. Pole-Zero Analysis

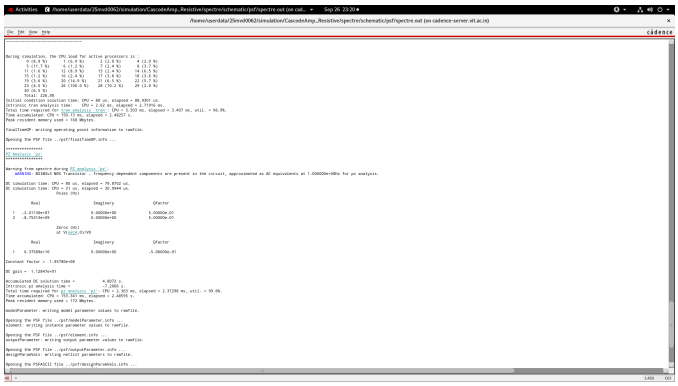

Fig. 10: Pole-zero analysis result

Pole-zero analysis provides detailed insight into the frequency stability and dominant dynamic behavior of the amplifier. The dominant pole located near the output node arises primarily from the load capacitance interacting with the effective output resistance of the cascode stage. Higher-order poles correspond to internal device capacitances and bias network nodes.

The separation between the dominant pole and the higher-frequency poles ensures a single-pole roll-off characteristic, which leads to improved stability margins and predictable transient response.

XIII. Transient Response Analysis

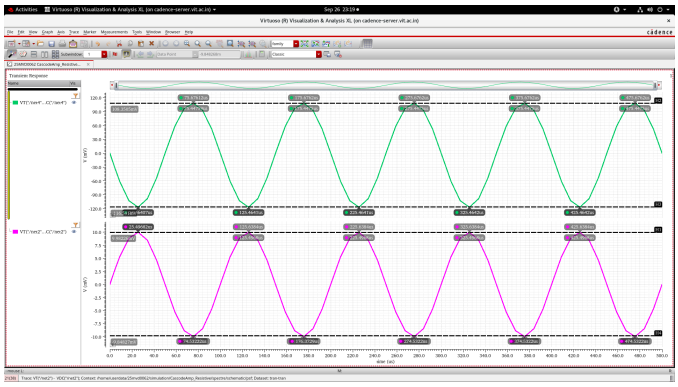

Fig. 11: Transient response of input and output signals

The transient waveform in Fig. 11 shows the sinusoidal input and the amplified output signal. The output waveform

exhibits a clear phase inversion relative to the input, consistent with the common-source operation of the input transistor. The absence of distortion in the output waveform indicates that the devices remain in the saturation region throughout the signal swing, validating the correctness of bias voltage selection.

XIV. Operating Point Verification

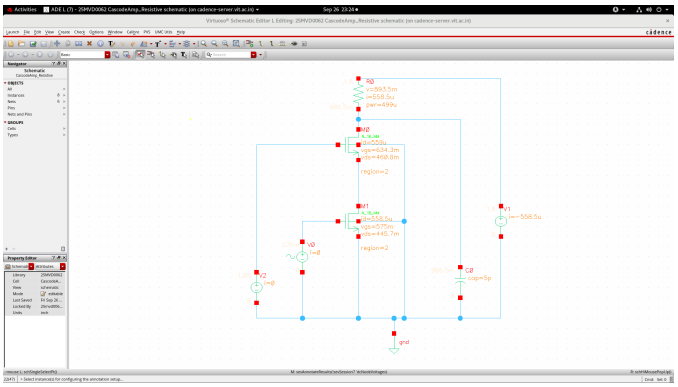

Fig. 12: DC operating point verification

The annotated schematic shows node voltages and operating regions of all transistors. Both NMOS devices operate in saturation, confirming that the gain predicted by small-signal analysis remains valid during actual circuit operation. Proper biasing also ensures maximum output swing without clipping.

XV. Nyquist Stability Analysis

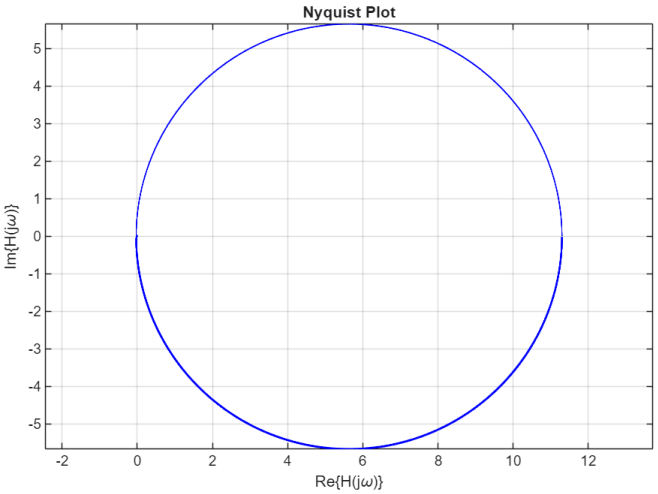

Fig. 13: Nyquist stability plot

The Nyquist plot in Fig. 13 illustrates the frequency-domain stability of the amplifier. Since the locus does not encircle the $(-1, 0)$ point, the system is unconditionally stable. The smooth elliptical shape indicates a well-damped system with adequate phase margin. Nyquist analysis complements Bode analysis by providing a graphical confirmation of closed-loop stability conditions.

XVI. Performance Summary

TABLE I: Performance Summary of Cascode Amplifier (Resistive Load)

Parameter	Value
Supply Voltage	1.8 V
Power Consumption	1 mW
Midband Gain	21.04 dB
Bandwidth	20 MHz
Unity Gain Frequency	229 MHz
Phase Margin	86.5°
Load Capacitance	5 pF

The results demonstrate that the designed amplifier satisfies the target gain, bandwidth, and power requirements while maintaining sufficient stability margin.

XVII. Discussion

The cascode topology significantly improves intrinsic gain by multiplying the output resistance of stacked transistors. Additionally, the reduced Miller capacitance enhances bandwidth, making the topology particularly suitable for high-speed analog applications such as RF receivers and high-resolution data converters.

The g_m/I_D methodology simplifies transistor sizing by allowing designers to directly select the desired inversion level without iterative calculations. This approach also improves portability of design methodology across different CMOS technology nodes.

XVIII. Cascode Amplifier with Current Source Load

While resistive loads provide simple implementation, current-source loads significantly increase voltage gain because they present a very high small-signal resistance at the output node. This section presents the design and analysis of the cascode amplifier using an active current-source load implemented with PMOS devices.

A. Operating Principle

In a current-source loaded cascode amplifier, the output node resistance is approximately

$$R_{out} \approx r_{oN} \parallel r_{oP} \tag{13}$$

where r_{oN} is the output resistance of the NMOS cascode stack and r_{oP} is the resistance of the PMOS current-source load. Since both resistances are large, the resulting effective output resistance becomes extremely high, producing very large intrinsic gain.

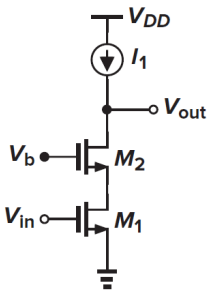

Fig. 14: Cascode amplifier with current-source load

B. Image Interpretation

The schematic in Fig. 14 shows the NMOS cascode input stage combined with a PMOS current mirror load. The PMOS devices act as active resistors whose incremental resistance can be several mega-ohms, much larger than a practical physical resistor in integrated circuits. This configuration enables gains exceeding 70 dB without consuming excessive silicon area.

XIX. Small-Signal Gain Analysis

The approximate gain of the current-source loaded cascode amplifier can be expressed as

$$A_v \approx g_{m1}(g_{m2}r_{o2})r_{o1}(r_{oP}) \tag{14}$$

Assuming large $g_m r_o$ products for both NMOS and PMOS devices, the gain can be simplified to

$$A_v \approx g_{m1}(g_{m2}r_{o1}r_{o2}) \tag{15}$$

This indicates that stacking devices dramatically multiplies the effective output resistance and therefore increases gain.

XX. PDM-Based Design Methodology

The PDM (Performance Driven Methodology) approach focuses on selecting transistor dimensions directly from required performance specifications such as gain, bandwidth, and bias current. Instead of relying solely on analytical equations, the method uses characterization curves extracted from the process design kit to determine device dimensions ensuring that all devices remain in saturation while meeting gain requirements.

A. NMOS Device Biasing

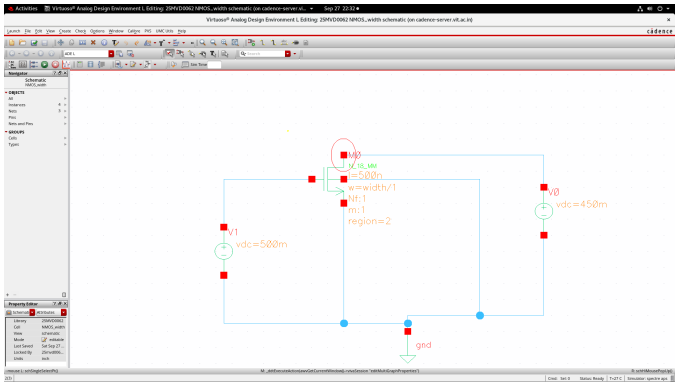

Fig. 15: Bottom NMOS characterization setup

The characterization setup sweeps gate voltage and extracts current density and operating region boundaries. Proper selection of gate bias ensures that the input transistor maintains sufficient overdrive voltage to handle signal swing without entering the triode region.

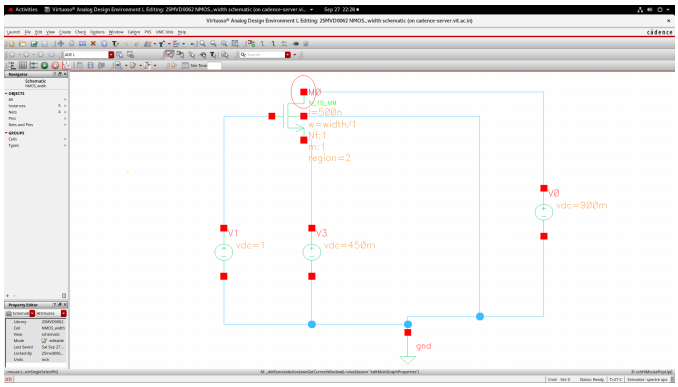

Fig. 16: Top NMOS cascode device characterization

The cascode device bias is chosen such that the drain voltage of the lower transistor remains nearly constant, thereby maximizing gain stability and minimizing channel-length modulation effects.

XXI. PMOS Current Source Design

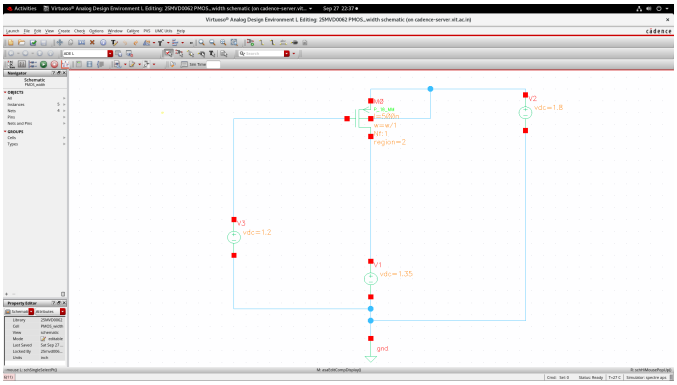

Fig. 17: Top PMOS current-source characterization

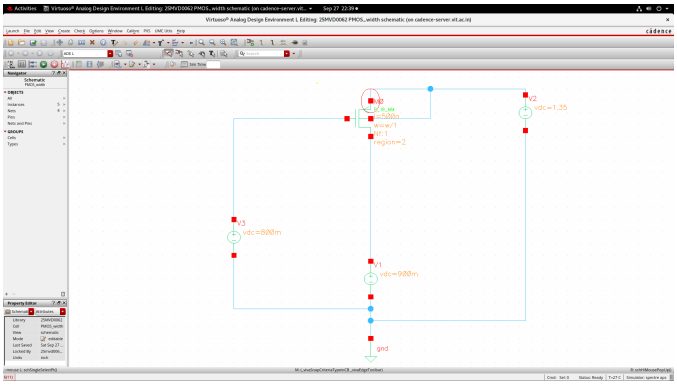

Fig. 18: Bottom PMOS bias device

PMOS devices operate as constant current sources whose small-signal resistance is inversely proportional to channel-length modulation. By selecting sufficiently long channel lengths, very high output resistance can be achieved, improving amplifier gain.

XXII. Complete Amplifier Implementation

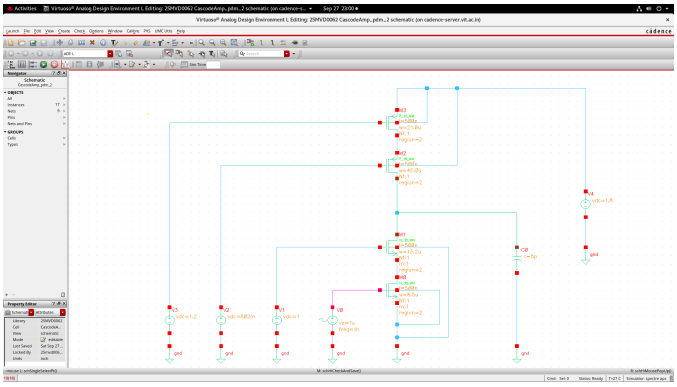

Fig. 19: Final cascode amplifier with current-source load

The final circuit integrates NMOS cascode devices and PMOS current mirror load to form a high-gain single-stage amplifier suitable for analog front-end applications.

XXIII. Comparison Between Resistive and Current-Source Loads

TABLE II: Comparison of Load Techniques

Parameter	Resistive Load	Current Source Load
Gain	Moderate	Very High
Output Resistance	Limited	Very High
Power Efficiency	Moderate	High
Chip Area	Larger (resistor area)	Smaller
Bias Complexity	Simple	Higher
Bandwidth	Higher	Slightly lower

From the comparison, current-source loading is preferred in high-gain analog stages, while resistive loading is used when simplicity and high bandwidth are required.

XXIV. Performance Summary (Current-Source Load)

TABLE III: Performance Summary of Cascode Amplifier (Current-Source Load)

Parameter	Value
Bias Current	20 μA
Gain	70.23 dB
Bandwidth	3.2 kHz
Unity Gain Frequency	10.25 MHz
Phase Margin	90.5°
Load Capacitance	5 pF

The results confirm that active current-source loading substantially increases gain while maintaining acceptable stability margins.

XXV. Extended Discussion

The results obtained from both amplifier implementations clearly demonstrate the fundamental trade-off between gain and bandwidth in analog circuit design. The resistive-load cascode amplifier achieves relatively high bandwidth because the load resistance is smaller, which reduces the RC time constant at the output node. However, the achievable gain is limited due to the finite value of the resistor.

In contrast, the current-source loaded cascode amplifier achieves extremely high voltage gain because the small-signal resistance of the PMOS current source is significantly larger than any practical on-chip resistor. This increased resistance leads to a higher output pole time constant, thereby reducing bandwidth. Such a trade-off is a fundamental design constraint in analog integrated circuits.

Another important observation from the design procedure is the effectiveness of the g_m/I_D methodology. By selecting a desired transconductance efficiency, designers can directly determine transistor dimensions without repeated iterative calculations. This approach greatly simplifies the design of modern CMOS analog circuits where accurate device models are available through characterization curves.

The PDM-based design used in the current-source load amplifier similarly enables performance-driven sizing. Instead of solving long analytical equations, transistor dimensions are chosen to directly meet performance targets such as gain, bias

current, and operating region constraints. This methodology improves design productivity and ensures robust operation across process variations.

XXVI. Design Insights

Several important insights can be drawn from the design and simulation results:

- Cascoding dramatically increases output resistance, which is the primary factor responsible for the high gain achieved in both amplifier designs.
- The Miller capacitance reduction provided by the cascode topology significantly enhances high-frequency performance.
- Proper bias voltage selection is critical to ensure that all transistors remain in saturation during signal swing, preventing gain degradation.
- Active current-source loading is preferred in high-gain analog front-end stages, whereas resistive loading is suitable for wideband amplifiers.
- The g_m/I_D methodology provides a scalable and technology-independent transistor sizing approach widely used in modern analog IC design.

XXVII. Future Scope

The cascode amplifier presented in this work can be further extended into advanced multi-stage amplifier architectures such as telescopic operational amplifiers and folded-cascode operational amplifiers. Future work may include:

- Layout-level implementation and post-layout parasitic extraction
- Noise performance analysis
- Mismatch and Monte Carlo simulations
- Low-voltage cascode design techniques for scaled technologies
- Compensation techniques for multi-stage amplifiers

Such extensions would enable the amplifier to be used in high-performance analog signal processing applications including data converters, RF receivers, and sensor interfaces.

XXVIII. Conclusion

This work presented the complete design, simulation, and performance evaluation of cascode amplifiers using both resistive-load and current-source load configurations. Theoretical analysis, transistor sizing using the g_m/I_D methodology, and Cadence-based simulations were used to verify the amplifier performance.

The resistive-load cascode amplifier achieved the specified bandwidth of 20 MHz while maintaining a gain of approximately 21 dB, demonstrating its suitability for high-speed applications. The current-source loaded cascode amplifier achieved a significantly higher gain of approximately 70 dB, confirming the advantage of active loads in high-gain analog stages.

Overall, the study confirms that cascode amplifier topologies remain fundamental building blocks in analog integrated circuit design due to their superior gain, improved stability, and scalable performance across CMOS technologies.

References

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[3] Cadence Design Systems, *Virtuoso Analog Design Environment User Guide*, Cadence Documentation.