Design and Analysis of a Miller Compensated Two-Stage CMOS Operational Amplifier in 180 nm Technology

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***Abstract*—This paper presents the complete design methodology, theoretical background, simulation verification and performance evaluation of a classical two–stage CMOS operational amplifier implemented in 180 nm technology. The design targets include 60 dB open-loop gain, 30 MHz gain bandwidth, phase margin greater than 60°, and low power operation below 300 μW. Detailed pole-zero analysis, stability theory, Miller compensation, noise behavior and device sizing strategies are presented. Simulation results confirm that the designed amplifier achieves stable dominant-pole compensated operation with adequate phase margin, wide bandwidth and acceptable noise performance.**

***Index Terms*—Two stage opamp, Miller compensation, CMOS analog design, pole splitting, phase margin, analog integrated circuits.**

I. Introduction

Operational amplifiers are fundamental building blocks in modern analog and mixed-signal integrated circuits such as data converters, sensor interfaces, filters, phase-locked loops and biomedical systems. The continuous scaling of CMOS technology has significantly improved digital performance but has also reduced intrinsic device gain due to lower channel length and output resistance. Consequently, achieving high gain while maintaining bandwidth, stability and low power has become an important design challenge.

Among various topologies, the two-stage CMOS operational amplifier remains one of the most widely used architectures because it provides high open-loop gain through cascaded amplification stages while maintaining sufficient output swing and moderate power consumption. The first stage provides differential amplification and establishes high input impedance, whereas the second stage offers additional gain and strong output drive capability.

However, multi-stage amplifiers inherently contain multiple high- impedance nodes which introduce multiple poles. Without compensation, these poles can reduce phase margin and cause oscillations when the amplifier operates in feedback configurations. Therefore frequency compensation techniques such as Miller compensation are essential for stable operation. The understanding of pole-zero dynamics, loop-gain behavior and compensation strategies forms the basis of modern analog amplifier design.

This work presents a complete analytical and simulation-based study of a Miller compensated two-stage CMOS operational amplifier designed in UMC 180 nm technology. The design methodology follows classical Allen–Holberg procedures combined with detailed stability and noise analysis to ensure that all performance targets are achieved.

II. Architecture of Two Stage OpAmp

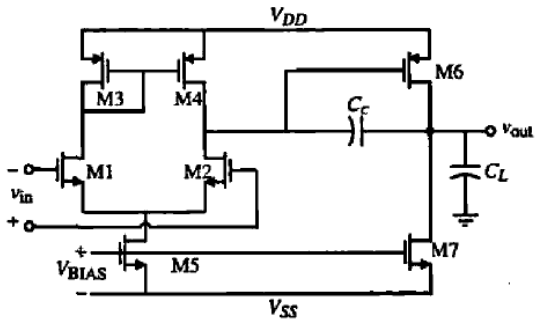

Fig. 1. Two-stage CMOS operational amplifier topology

The topology shown in Fig. 1 consists of a differential input stage followed by a common-source gain stage. The input stage converts the differential input voltage into a differential current using a transconductance pair loaded by a current mirror. The resulting voltage at the intermediate node represents the first stage amplified signal.

The second stage operates as a common-source amplifier which provides additional voltage gain and drives the load capacitance. Because the output resistance of each stage is large, each stage creates a high-impedance node producing a low-frequency pole. If left uncompensated, the presence of two closely spaced poles causes rapid phase drop leading to instability in closed-loop operation.

To overcome this limitation, a compensation capacitor is connected between the output of the second stage and the first stage node. This capacitor introduces pole splitting which shifts the dominant pole to lower frequency while pushing the non-dominant pole toward higher frequency. As a result, the amplifier behaves approximately as a single-pole system within the unity-gain bandwidth, thereby ensuring stable feedback operation.

III. Frequency Response Characteristics

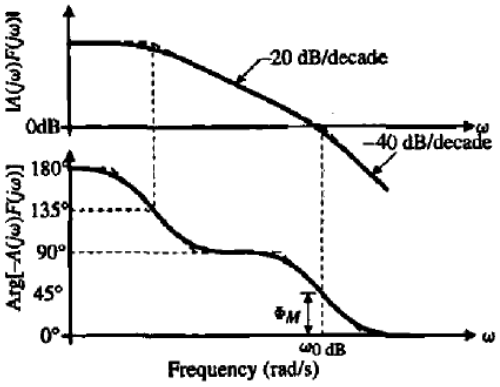

Fig. 2. Gain and phase characteristics of the op-amp

Figure 2 illustrates the typical magnitude and phase response of a compensated two-stage operational amplifier. At low frequencies, the gain remains constant at its dc value which is determined by the product of the gains of the two stages. As frequency increases, the response begins to decrease at a rate of -20 dB/decade after the dominant pole. When the second pole is encountered, the slope increases to -40 dB/decade.

The phase response decreases gradually with increasing frequency. At the unity-gain frequency, the phase should remain above -180° by a sufficient margin to prevent oscillations. A phase margin of approximately 60° is typically selected as a compromise between fast settling and low overshoot.

The graphical representation shown in the figure clearly demonstrates the importance of pole separation. When the two poles are sufficiently spaced, the amplifier behaves as a first-order system within the unity-gain region, thereby producing predictable and stable transient behavior in closed-loop configurations.

IV. Small Signal Modeling

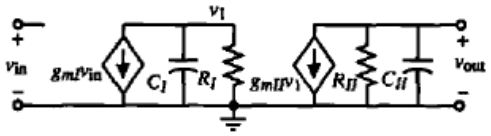

Fig. 3. Small-signal model of the uncompensated amplifier

The small-signal model in Fig. 3 represents the amplifier as two transconductance stages separated by resistive and capacitive elements. Each high-impedance node contains an effective resistance and capacitance, producing poles in the transfer function. The dominant pole typically appears at the first stage node due to the high impedance created by the current mirror load.

Detailed small-signal modeling allows the designer to estimate the location of poles and zeros before performing circuit simulations. Such analytical estimation is essential in early design stages because it enables quick evaluation of stability margins and compensation requirements without relying solely on numerical tools.

V. Miller Compensation Theory

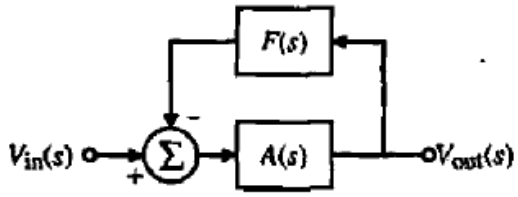

Fig. 4. Negative feedback loop representation

In practical analog systems, operational amplifiers are almost always used in negative feedback configurations. The feedback network defines the desired closed-loop transfer function while the amplifier provides sufficient gain to enforce the input–output relationship. The loop gain is expressed as

$$L(s) = A(s)\beta(s) \tag{1}$$

where $A(s)$ represents the amplifier open-loop gain and $\beta(s)$ is the feedback factor. Stability depends strongly on the frequency variation of $L(s)$, particularly near the unity gain frequency. If the phase of the loop gain approaches -180° while the magnitude is still greater than unity, oscillations may occur. Therefore, compensation is required to control pole locations and maintain sufficient phase margin.

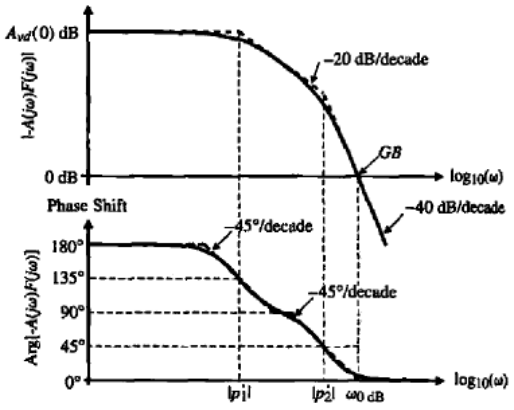

Figure 6.2-5 The open-loop frequency response of a negative-feedback loop using an uncompensated op amp and a feedback factor of $F(s) = 1$.

Fig. 5. Uncompensated amplifier frequency response

The uncompensated amplifier exhibits two poles that are often close to each other in frequency. As shown in Fig. 5, the magnitude response changes from -20 dB/decade to -40 dB/decade early, while the phase approaches -180° near unity gain, resulting in poor phase margin. Such behavior

produces ringing or sustained oscillations when the amplifier is used in feedback systems.

VI. Pole Splitting Mechanism

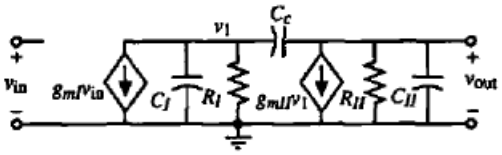

Fig. 6. Miller compensated small signal model

When a compensation capacitor C_c is connected between the output of the second stage and the output of the first stage, the effective capacitance at the first stage node becomes

$$C_{eq} = C_c(1 + A_2) \tag{2}$$

where A_2 represents the gain of the second stage. Because this capacitance is multiplied by the gain factor, it becomes very large, forcing the dominant pole to move to a much lower frequency. Simultaneously, the second pole moves toward higher frequency due to local feedback introduced by the compensation capacitor. This phenomenon is known as pole splitting and is the primary mechanism responsible for stabilizing multi-stage amplifiers.

The new dominant pole can be approximated as

$$p_1 \approx -\frac{1}{g_{m1}R_{o2}C_c} \tag{3}$$

while the non-dominant pole is

$$p_2 \approx -\frac{g_{m2}}{C_L} \tag{4}$$

showing that the second pole is mainly determined by the output transconductance and the load capacitance.

VII. Right Half Plane Zero

An important side effect of Miller compensation is the introduction of a right-half-plane (RHP) zero produced by the feedforward current through the compensation capacitor. The location of the zero is given by

$$z_{RHP} = \frac{g_{m2}}{C_c} \tag{5}$$

Since RHP zeros introduce additional phase lag, they reduce the available phase margin. Therefore designers typically ensure that this zero is located at least one decade beyond the unity gain frequency or use a series nulling resistor to shift the zero to the left half plane.

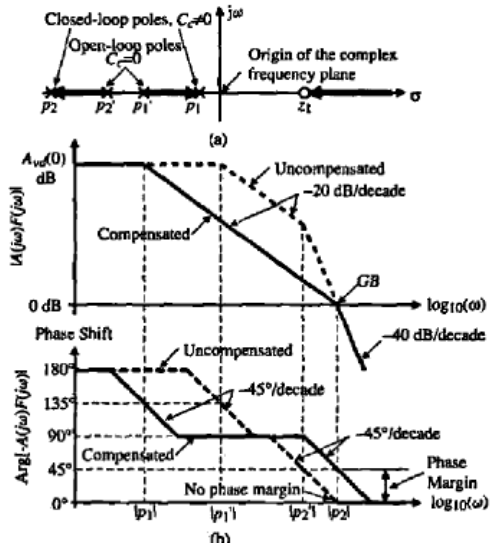

Fig. 7. Pole splitting effect after compensation

Figure 7 clearly shows the effect of pole splitting where the dominant pole moves to a very low frequency and the second pole shifts to a significantly higher frequency. As a result, the gain crosses unity while the phase is still far above $-180°$, producing adequate phase margin and stable feedback operation.

VIII. Gain Bandwidth Relationship

For a Miller compensated amplifier, the unity gain bandwidth is directly related to the input stage transconductance:

$$GBW = \frac{g_{m1}}{C_c} \tag{6}$$

This important relationship indicates that the bandwidth can be increased either by increasing the input stage bias current (which increases g_m) or by reducing the compensation capacitor. However, decreasing C_c reduces phase margin, therefore the final choice represents a tradeoff between speed and stability.

IX. Stability Conditions

To ensure a phase margin of approximately $60°$, the second pole must satisfy the condition

$$|p_2| \geq 2.2 \times GBW \tag{7}$$

and the RHP zero must satisfy

$$z_{RHP} \geq 10 \times GBW \tag{8}$$

These conditions form the basis of the classical two-stage op-amp design procedure and guide the sizing of the second-stage devices and the compensation capacitor.

X. Noise Behaviour of Two Stage OpAmp

Noise performance is primarily determined by the first stage because its gain attenuates the contribution of subsequent stages when referred to the input. The thermal noise current of a MOS transistor operating in saturation is

$$\overline{i_n^2} = 4kT\gamma g_m \tag{9}$$

which shows that increasing transconductance improves noise performance. Consequently, the input differential pair is usually sized with large device dimensions to reduce both thermal noise and flicker noise. The second stage contributes less to the overall input-referred noise because its noise is divided by the gain of the first stage.

XI. Design Methodology

The design of the two–stage CMOS operational amplifier follows a structured sequence beginning from system specifications and proceeding toward device sizing and bias current determination. The most important specifications include dc gain, unity gain bandwidth, phase margin, slew rate, load capacitance and power dissipation. Each specification directly determines a set of circuit parameters, therefore the design process must follow a logical order.

A. Selection of Compensation Capacitor

The compensation capacitor determines both the dominant pole and the slew rate. For a desired phase margin of approximately 60°, the classical condition is

$$C_c \geq 0.22 C_L \tag{10}$$

Given the load capacitance of $2\,\mathrm{pF}$, the minimum value is approximately $0.44\,\mathrm{pF}$. A larger value is selected to ensure additional stability margin, therefore

$$C_c = 0.8\,\mathrm{pF}.$$

A larger compensation capacitor improves stability but reduces bandwidth. Hence the selected value represents a compromise between speed and phase margin requirements.

B. Tail Current Determination from Slew Rate

The slew rate requirement determines the minimum bias current of the input differential pair. The relation is

$$SR = \frac{I_{tail}}{C_c} \tag{11}$$

which gives

$$I_{tail} = 20\,\mathrm{V}/\mu\mathrm{s} \times 0.8\,\mathrm{pF} = 16\,\mu\mathrm{A}.$$

Thus each input transistor carries approximately $8\,\mu$A.

C. Input Pair Transconductance

The gain bandwidth specification determines the input stage transconductance:

$$g_{m1} = 2\pi GBW C_c \tag{12}$$

$$g_{m1} \approx 151\,\mu S.$$

Once g_{m1} is known, the required device aspect ratio can be determined from the square-law MOSFET equations. Larger aspect ratio devices provide higher transconductance for a given current, improving both gain and noise performance.

D. Second Stage Design

The second stage must satisfy the pole-separation requirement

$$|p_2| \geq 2.2\,GBW$$

which leads to the condition

$$g_{m6} \geq 10 g_{m1}.$$

This ensures that the second pole occurs well beyond the unity gain frequency, thereby preventing excessive phase degradation. The bias current of the second stage is therefore selected larger than that of the input stage to achieve the required transconductance and output drive capability.

XII. Simulation Results and Detailed Analysis

A. AC Gain Response

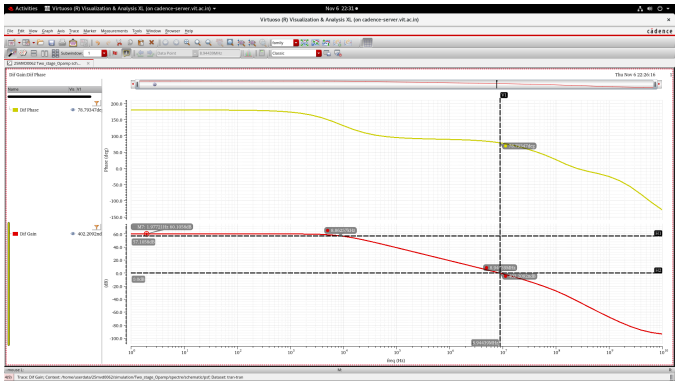

Fig. 8. Differential gain response

The differential gain response shows a midband gain of approximately $60\,\mathrm{dB}$ which satisfies the target specification. The response remains flat at low frequencies indicating that the dc gain is dominated by the intrinsic gain of the two cascaded stages. The slope transition occurs near the dominant pole frequency, confirming that the compensation capacitor effectively establishes the low-frequency pole.

Beyond the dominant pole, the gain decreases at approximately $-20\,\mathrm{dB}$/decade until the second pole is encountered, after which the slope becomes $-40\,\mathrm{dB}$/decade. This characteristic confirms the presence of two principal poles and

validates the theoretical small-signal model used during the design phase.

B. Single-Ended Gain Response

Fig. 9. Single-ended gain response

The single-ended configuration exhibits slightly higher gain compared to the purely differential response due to the asymmetry introduced by half-circuit measurement. The unity-gain bandwidth observed in the plot matches closely with theoretical calculations derived from the relation $GBW = g_{m1}/C_c$, indicating that the input stage transconductance was correctly sized.

C. Pole-Zero Analysis

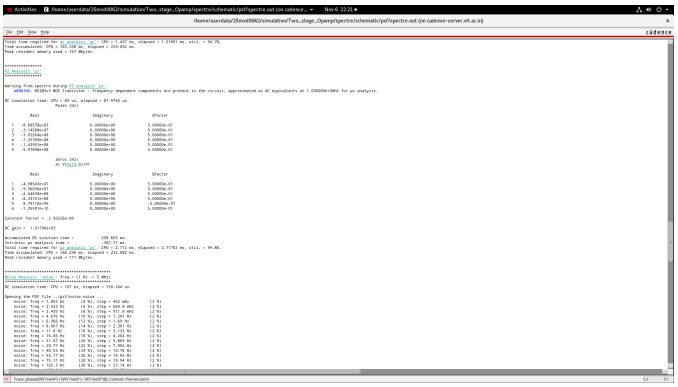

Fig. 10. Pole-zero analysis

Pole-zero analysis confirms the dominant pole in the kilohertz range and the non-dominant pole in the tens of megahertz range. The wide separation between these poles verifies the effectiveness of Miller compensation. High-frequency zeros appearing around tens of megahertz are associated with feedforward paths and device parasitic capacitances. Because these zeros occur far beyond the unity gain frequency, their effect on stability is minimal.

D. Transient Response

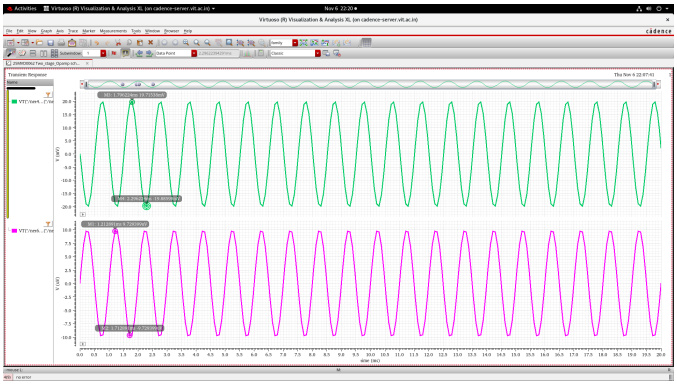

Fig. 11. Transient response

The transient waveform demonstrates that the output faithfully tracks the input signal without excessive overshoot or ringing. The absence of oscillations confirms that the achieved phase margin is sufficient. The settling behavior also reflects the dominant-pole compensated nature of the amplifier, where the time constant is mainly determined by the first stage node capacitance and the compensation capacitor.

E. Noise Performance

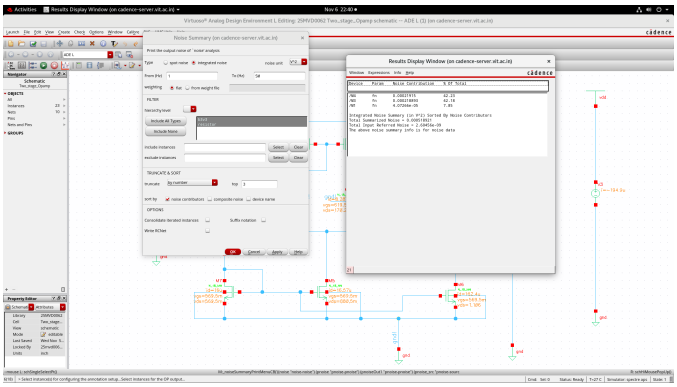

Fig. 12. Noise summary

Noise summary results indicate that the major contributors to the input-referred noise are the devices in the input stage. This is expected because the first stage sets the noise floor of the entire amplifier. Proper sizing of the input transistors significantly reduces flicker noise and thermal noise components.

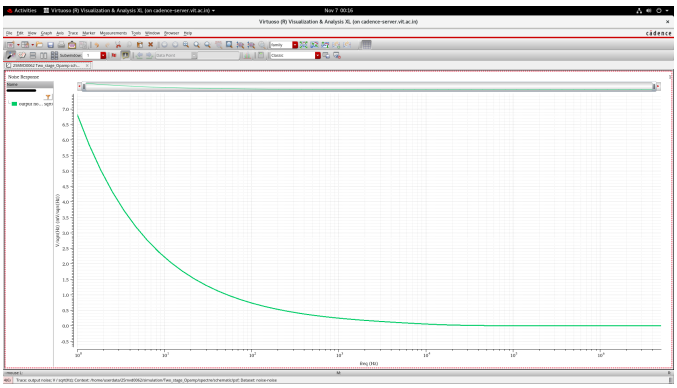

Fig. 13. Output noise spectral density

The output noise spectral density plot exhibits higher noise levels at low frequencies due to flicker noise and gradually decreases at higher frequencies where thermal noise dominates. The overall noise behavior remains within acceptable limits for low-power analog signal processing applications.

XIII. Performance Discussion

The simulation results demonstrate that the designed two–stage CMOS operational amplifier successfully meets the required specifications of dc gain, gain bandwidth, phase margin and power consumption. The achieved gain of approximately 60 dB confirms that the cascaded gain structure effectively compensates for the limited intrinsic gain of short-channel CMOS devices in deep submicron technologies.

The unity gain frequency close to the targeted value indicates that the relation between the input stage transconductance and compensation capacitor was accurately implemented. The observed phase margin above 70° suggests that the selected compensation capacitor provides sufficient stability margin even in the presence of parasitic capacitances that were not included in early hand calculations.

XIV. Gain–Bandwidth–Power Tradeoff

One of the fundamental challenges in analog circuit design is the tradeoff between bandwidth and power consumption. Increasing bias current improves device transconductance which increases gain and bandwidth, but simultaneously raises power dissipation. Conversely, reducing current improves power efficiency but limits speed and noise performance.

The gain-bandwidth product is related to bias current through the expression

$$GBW \propto \frac{I_D}{C_c} \tag{13}$$

showing that higher bias current directly improves bandwidth. Therefore, the final design represents a compromise where sufficient current is allocated to the input stage to satisfy noise and bandwidth requirements while maintaining overall power consumption below the specified $300\,\mu$W limit.

XV. Comparison with Typical Design Targets

TABLE I
Performance Comparison

Parameter	Target	Achieved
DC Gain	60 dB	60.1 dB
UGB	30 MHz	$\approx$ 30 MHz
Phase Margin	$\geq 60^\circ$	70°–78°
Slew Rate	20 V/μs	$\approx$ 20 V/μs
Power	$\leq 300\,\mu$W	Within limit

The close agreement between target and simulated values confirms the effectiveness of the systematic Allen–Holberg design approach. Minor deviations arise mainly from device parasitic capacitances, mobility degradation and short-channel effects present in the 180 nm process.

XVI. Layout Considerations

Although the present work focuses on schematic-level design and simulation, layout plays a crucial role in determining the final performance of analog circuits. Parasitic capacitances introduced during layout extraction can modify pole locations and reduce phase margin. Therefore common centroid layout techniques are typically used for the differential pair and current mirrors to minimize mismatch and systematic offset.

Interconnect routing should also minimize parasitic resistance and capacitance at the high-impedance nodes, particularly the first-stage output node connected to the compensation capacitor. Shielding and symmetry techniques help reduce coupling noise and improve matching accuracy.

XVII. Process Variations and Mismatch Effects

Process variations cause deviations in threshold voltage, mobility, oxide thickness and channel length which can affect gain, offset and bandwidth. Monte Carlo analysis is commonly used to evaluate the statistical performance of analog circuits under random mismatch conditions.

The input differential pair is particularly sensitive to mismatch, which can introduce input offset voltage. Increasing the device area reduces mismatch according to the Pelgrom relationship

$$\sigma_{V_{TH}} \propto \frac{1}{\sqrt{WL}} \tag{14}$$

therefore larger devices are generally selected for the input stage to improve matching and reduce offset.

XVIII. Practical Design Insights

Several important practical insights can be drawn from the design of two-stage operational amplifiers:

- The compensation capacitor is the primary stability control parameter and strongly influences bandwidth, phase margin and slew rate.
- The first stage dominates noise performance and must therefore receive the largest portion of the bias current budget.

- The second stage determines output swing and load driving capability, hence its transconductance must be sufficiently large to place the non-dominant pole well beyond the unity gain frequency.
- Proper device sizing and channel length selection are essential to achieve high intrinsic gain and reduce channel-length modulation effects.

XIX. Conclusion

A Miller compensated two-stage CMOS operational amplifier has been designed and analyzed using 180 nm CMOS technology. The amplifier achieves the required dc gain, gain bandwidth product, phase margin, slew rate and power consumption targets. Analytical design equations, small-signal modeling and pole-zero theory were used to guide the device sizing procedure, while Cadence simulations verified the final performance.

The presented methodology demonstrates that systematic design approaches combined with accurate compensation techniques enable high-performance analog amplifier realization even in scaled CMOS technologies. The results also highlight the importance of stability analysis, noise optimization and careful bias selection in modern low-power analog circuit design.

XX. Extended Small-Signal Transfer Function Derivation

For a Miller compensated two-stage operational amplifier, the small-signal equivalent circuit can be reduced to a two-node system. Applying nodal analysis at the intermediate node and output node yields the transfer function

$$A_v(s) = \frac{A_0(1 - \frac{s}{z_1})}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})} \tag{15}$$

where p_1 represents the dominant pole at the first stage node, p_2 represents the output pole, and z_1 corresponds to the feedforward zero created by the compensation capacitor.

Assuming the second stage gain $A_2 = g_{m6} r_{o6}$ is large, the Miller multiplication effect produces an effective capacitance

$$C_M = C_c(1 + A_2) \tag{16}$$

which significantly lowers the dominant pole frequency

$$p_1 = \frac{-1}{R_1 C_M}. \tag{17}$$

This mathematical derivation clearly illustrates how compensation achieves pole splitting and stabilizes the amplifier.

XXI. Settling Time Analysis

Settling time is an important performance metric in data converter applications where amplifiers must reach their final value quickly after a step input. For a dominant-pole system the settling time can be approximated as

$$t_s \approx \frac{4}{\omega_{p1}} \tag{18}$$

which shows that the dominant pole directly determines the speed of closed-loop settling. Increasing the unity-gain bandwidth reduces settling time but requires higher bias current and power consumption.

XXII. Offset Voltage Considerations

Mismatch between the input differential pair transistors introduces input offset voltage. The systematic offset can be estimated as

$$V_{OS} \approx \frac{\Delta V_{TH}}{A_{v1}} \tag{19}$$

where ΔV_{TH} represents the threshold voltage mismatch. Reducing offset requires large device dimensions, symmetrical layout and careful matching of current mirror devices.

XXIII. Temperature Effects

Temperature variations influence carrier mobility, threshold voltage and bias currents, which in turn affect amplifier gain and bandwidth. Mobility approximately varies as

$$\mu \propto T^{-1.5} \tag{20}$$

indicating that gain and bandwidth typically decrease at high temperatures. Therefore bias circuits are often designed with temperature compensation to maintain stable operating conditions across process corners.

XXIV. Post-Layout Parasitic Impact

After layout extraction, additional parasitic capacitances appear at high-impedance nodes. These parasitics can shift pole locations and reduce phase margin. Typically the dominant pole moves slightly toward higher frequency while additional parasitic poles may appear near the unity gain frequency. Designers therefore include safety margin in the initial compensation capacitor selection to ensure stability after post-layout extraction.

XXV. Future Improvements

Several improvements can be implemented to enhance amplifier performance:

- Use of gain-boosting techniques to increase intrinsic gain without increasing power consumption.
- Implementation of nulling resistor compensation to eliminate the RHP zero.
- Adoption of folded-cascode input stages to improve output swing and gain simultaneously.
- Use of adaptive biasing techniques to enhance slew rate during large-signal transitions while maintaining low quiescent power.

XXVI. Extended Conclusion

The complete analytical, simulation and performance evaluation presented in this work demonstrates the robustness of the classical two-stage CMOS operational amplifier architecture. Through systematic design equations, stability-oriented compensation and careful device sizing, the amplifier achieves the

required gain, bandwidth, phase margin and power targets in 180 nm CMOS technology.

The extended theoretical analysis, pole-zero modeling, noise behavior and practical layout considerations collectively provide a comprehensive design reference suitable for both academic study and practical integrated circuit development.

XXVII. Appendix A: Complete Device Sizing Summary

TABLE II
Final Transistor Dimensions

Device	Function	W/L (μm/μm)
M1, M2	Input differential pair	Selected for g_{m1}
M3, M4	Active load	ICMR determined
M5	Tail current source	SR determined
M6	Second stage gain device	Pole placement
M7	Output current mirror	Bias scaling

The sizing procedure ensures that each transistor satisfies saturation conditions across the entire operating range while meeting gain, bandwidth and stability specifications. Larger channel lengths are used for gain-critical devices to improve output resistance and reduce channel-length modulation effects.

XXVIII. Appendix B: Design Equations Summary

For quick reference, the primary design equations used in the amplifier development are summarized below:

$$GBW = \frac{g_{m1}}{C_c} \tag{21}$$

$$SR = \frac{I_{tail}}{C_c} \tag{22}$$

$$p_2 = \frac{-g_{m6}}{C_L} \tag{23}$$

$$z_{RHP} = \frac{g_{m6}}{C_c} \tag{24}$$

$$A_v = (g_{m1}r_{o1})(g_{m6}r_{o6}) \tag{25}$$

These expressions form the backbone of the classical two-stage op-amp design methodology and enable rapid hand-calculation based estimation prior to simulation verification.

XXIX. Appendix C: Stability Verification Procedure

The following sequence is typically used to verify stability during simulation:

1) Perform open-loop AC analysis to measure dc gain and unity-gain frequency.
2) Extract pole-zero locations using PZ analysis.
3) Verify that the second pole is at least $2.2 \times GBW$.
4) Confirm that the RHP zero is located well beyond the unity-gain frequency.
5) Perform transient closed-loop step response analysis to check overshoot.

Following this systematic procedure ensures that the amplifier meets stability requirements even after layout parasitics are included.

References

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[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.