Fin-FET and GAAFET

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***Abstract*—This study presents a comparative TCAD-based evaluation of p-type Fin Field-Effect Transistor (FinFET) and Gate-All-Around Field-Effect Transistor (GAAFET) structures to assess their short-channel performance at sub-45 nm technology nodes. Both devices were designed and simulated using Synopsys Sentaurus TCAD under identical material and process conditions to ensure a consistent and unbiased comparison. The FinFET model features a fin width of 7 nm and a fin height of 22 nm, whereas the GAAFET incorporates a nanowire channel with $W = H = 7$ nm, providing complete gate encapsulation for enhanced electrostatic control. Simulations were conducted across gate lengths ranging from 12 nm to 45 nm, and key performance parameters—including ON current (I_{on}), OFF current (I_{off}), subthreshold swing (SS), and drain-induced barrier lowering (DIBL)—were extracted from the transfer characteristics.**

The simulation outcomes indicate that the p-type GAAFET demonstrates superior electrostatic integrity compared to the FinFET, achieving a lower subthreshold swing of approximately 60 mV/dec, a smaller DIBL of around 1000 mV/V, and an enhanced I_{on}/I_{off} ratio exceeding 10^7. These results highlight that the GAAFET architecture offers improved gate control, reduced short-channel effects, and better energy efficiency, making it a strong candidate for future low-power CMOS technology nodes.

***Index Terms*—PMOS, FinFET, GAAFET, TCAD Simulation, Subthreshold Swing, DIBL, Short-Channel Effects, Device Scaling, Low-Power CMOS**

I. Introduction

The ongoing downscaling of complementary metal–oxide–semiconductor (CMOS) technology has driven significant advancements in device performance, integration density, and power efficiency. However, as transistor dimensions shrink below the 45 nm node, conventional planar MOSFETs encounter pronounced short-channel effects (SCEs) such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and elevated leakage currents. These effects degrade the device's switching behavior and impose fundamental limitations on the continued scaling of traditional planar transistor architectures.

To address these challenges, advanced multi-gate transistor architectures such as the Fin Field-Effect Transistor (FinFET) have been developed. In a FinFET, the channel is formed by a thin, vertical fin structure, enabling the gate to exert control over multiple sides of the channel simultaneously. This three-dimensional design significantly enhances electrostatic control, minimizes leakage currents, and increases drive strength when compared to traditional planar MOSFETs. However, as device dimensions approach the sub-10 nm scale, FinFETs encounter inherent limitations such as corner effects and non-uniform channel inversion, which hinder their scalability and overall performance at extreme miniaturization levels.

The Gate-All-Around Field-Effect Transistor (GAAFET) has emerged as an evolution of the FinFET, offering complete gate control around the channel. The GAAFET's cylindrical or nanowire-type structure provides superior electrostatic integrity, minimal leakage, and near-ideal subthreshold swing (SS) characteristics. This makes it a promising candidate for future low-power, high-performance CMOS applications.

In this work, a detailed TCAD-based analysis of p-type FinFET and GAAFET devices is performed using Synopsys Sentaurus. Both devices are modeled with equivalent material and doping parameters to ensure a fair comparison. The objective is to investigate the effect of device geometry on short-channel parameters such as ON-current (I_{on}), OFF-current (I_{off}), subthreshold swing (SS), and DIBL across different gate lengths (12 nm – 45 nm). The simulation results demonstrate that the GAAFET exhibits superior electrostatic control and reduced short-channel effects compared to the FinFET, confirming its suitability for future nanoscale CMOS technologies.

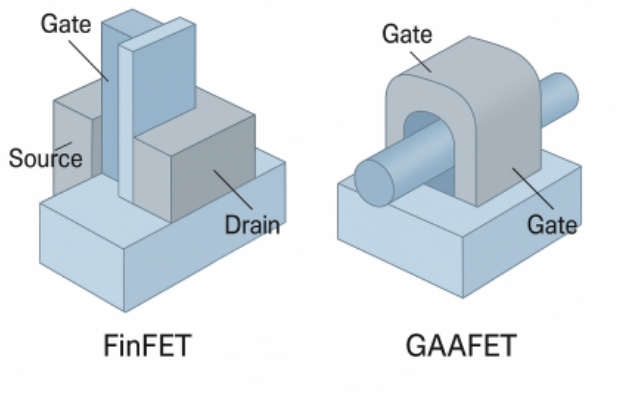

Fig. 1: FinFET and GAAFET (placeholder). Replace with actual figure.

II. Background Theory

As CMOS technology continues to scale below the 45 nm node, the control of the channel potential by the gate weakens

due to increased drain-to-channel coupling. This phenomenon gives rise to several short-channel effects (SCEs), including DIBL, threshold voltage roll-off, and elevated subthreshold leakage currents. These effects adversely impact device reliability, power efficiency, and switching performance in traditional planar MOSFETs.

To address these challenges, three-dimensional (3D) multi-gate structures such as the FinFET and GAAFET have been developed. These structures improve the gate-to-channel coupling by increasing the gate's control area around the channel, thereby reducing electrostatic interference from the drain.

In the FinFET, the gate wraps around three sides of a vertical silicon fin. The effective channel width of a FinFET can be expressed as:

$$W_{\text{eff}} = 2H_{\text{fin}} + W_{\text{fin}} \tag{1}$$

where H_{fin} and W_{fin} are the fin height and fin width, respectively.

The GAAFET completely surrounds the channel with the gate electrode. For a square or circular nanowire, an effective width approximation is:

$$W_{\text{eff}} = 4W \tag{2}$$

where W is the channel dimension.

The subthreshold swing (SS) and drain-induced barrier lowering (DIBL) quantify gate control and drain coupling:

$$\text{SS} = \left(\frac{dV_G}{d(\log I_D)} \right) \times 1000 \text{ [mV/dec]} \tag{3}$$

$$\text{DIBL} = \frac{V_{th,\text{low}} - V_{th,\text{high}}}{V_{DS,\text{high}} - V_{DS,\text{low}}} \times 1000 \text{ [mV/V]} \tag{4}$$

III. Simulation Framework

The simulation and analysis of the p-type FinFET and GAAFET devices were carried out using the Synopsys Sentaurus TCAD suite. The process consists of: structure creation (using Sentaurus Structure Editor, SDE), physical modeling, and electrical characterization (Sentaurus Device).

A. Structure Creation

The FinFET structure was designed with:

- $W_{\text{fin}} = 7$ nm, $H_{\text{fin}} = 22$ nm,
- gate lengths L_g of 12, 16, 22, 32 and 45 nm.

The GAAFET used a square nanowire channel with $W = H = 7$ nm and the same L_g values. Both devices used a 2 nm SiO_2 gate oxide and metal gate (work function 4.6 eV). Doping: source/drain n^+ 4×10^{19} cm^{-3}, channel p-type 8×10^{15} cm^{-3}, substrate p-type 1×10^{15} cm^{-3}.

B. Physical Models

Drift-diffusion transport model was used with:

- Doping-dependent mobility and high-field saturation,
- Lombardi surface mobility,
- SRH and Auger recombination,
- Bandgap narrowing and Fermi-Dirac statistics,
- Quantum correction for narrow-channel confinement.

C. Electrical Simulation and Parameter Extraction

DC simulations produced transfer (I_D–V_G) and output (I_D–V_D) characteristics. For p-type operation gate voltage was swept from 0 V to -1 V; drain varied between -0.05 V and -0.3 V.

Threshold voltage V_{th} extraction used the constant-current method:

$$I_{\text{ref}} = 1 \times 10^{-7} \times \frac{W_{\text{eff}}}{L_g} \tag{5}$$

with $W_{\text{eff}} = 2H_{\text{fin}} + W_{\text{fin}}$ for FinFET and $W_{\text{eff}} = 4W$ for GAAFET. SS was taken from the slope of $\log I_D$ vs V_G, and DIBL from V_{th} shift between $V_{DS} = 0.05$ V and 0.3 V. I_{on} at $V_G = V_{DD}$ and I_{off} at $V_G = 0$ V.

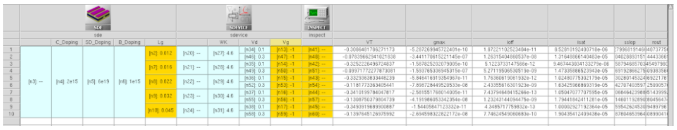

Fig. 2: FinFET Work Bench.

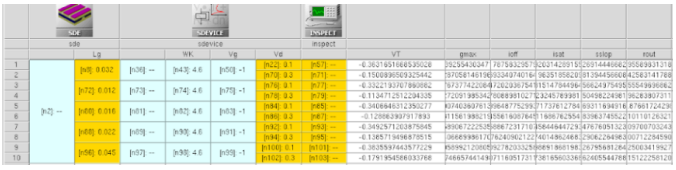

Fig. 3: GAAFET Work Bench

IV. Theoretical Calculations

A. Threshold Voltage

The long-channel threshold voltage under zero substrate bias:

$$V_{th} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{6}$$

with body effect coefficient

$$\gamma = \sqrt{\frac{2q\varepsilon_{Si}N_A}{C_{ox}}}, \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}. \tag{7}$$

B. Subthreshold Swing

SS definition repeated:

$$\text{SS} = \left(\frac{dV_G}{d(\log I_D)} \right) \times 1000 \text{ [mV/dec]} \tag{8}$$

The theoretical minimum SS at 300 K is:

$$\text{SS}_{\min} = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right). \tag{9}$$

C. DIBL

DIBL:

$$\text{DIBL} = \frac{V_{th,\text{low}} - V_{th,\text{high}}}{V_{DS,\text{high}} - V_{DS,\text{low}}} \times 1000 \text{ [mV/V]}. \tag{10}$$

D. ON/OFF Currents

The relation for Ion/Ioff ratio approximate dependence:

$$\frac{I_{\text{on}}}{I_{\text{off}}} \propto \exp\left(\frac{V_{DD} - V_{th}}{\text{SS}}\right). \tag{11}$$

V. Simulation Results and Discussion

A. Device Structure

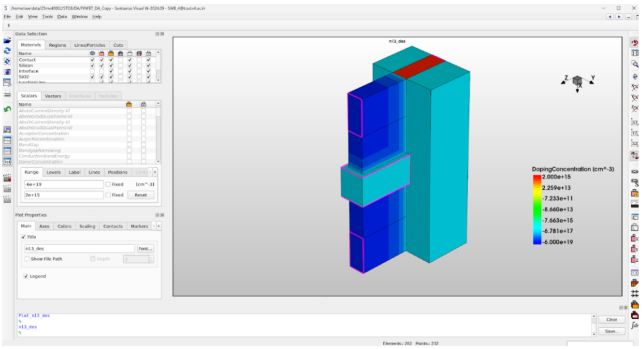

Fig. 4: 3D structure: FinFET.

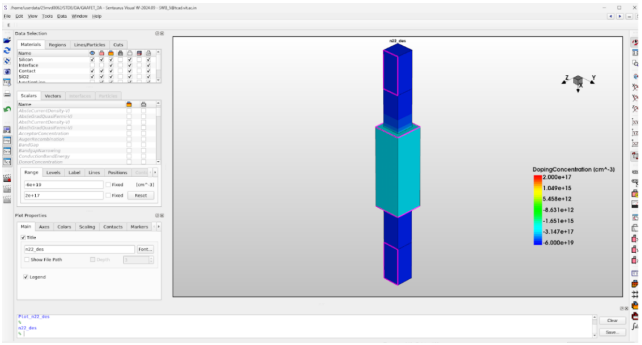

Fig. 5: 3D structure: GAAFET.

For the simulated FinFET: $W_{\text{fin}} = 7$ nm, $H_{\text{fin}} = 22$ nm so

$$W_{\text{eff}} = 2H_{\text{fin}} + W_{\text{fin}} = 2 \times 22 + 7 = 51 \text{ nm}. \tag{12}$$

For the GAAFET: $W = H = 7$ nm so

$$W_{\text{eff}} = 4W = 28 \text{ nm}. \tag{13}$$

B. Threshold Voltage and DIBL

Table IV lists the extracted V_{th} at $V_{DS} = 0.1$ V and 0.3 V, along with the computed DIBL. The GAAFET maintains a DIBL near 1000 mV/V across all gate lengths—roughly half that of the FinFET.

C. Subthreshold Swing (SS)

SS was extracted using two current levels $I_{D1} = 10^{-8}$ A and $I_{D2} = 10^{-9}$ A:

$$\text{SS} = \frac{V_{G1} - V_{G2}}{\log(I_{D1}) - \log(I_{D2})}. \tag{14}$$

GAAFET achieves lower SS (≈ 60 mV/dec) for several L_g values, approaching the thermal limit of 60 mV/dec at 300 K.

TABLE I: Extracted Subthreshold Swing (SS) for PMOS FinFET and GAAFET Devices

L_g (nm)	Device	SS (mV/dec)
12	FinFET	89.371
16	FinFET	81.616
22	FinFET	77.082
32	FinFET	73.695
45	FinFET	71.726
12	GAAFET	84.057
16	GAAFET	78.899
22	GAAFET	75.188
32	GAAFET	72.435
45	GAAFET	71.957

D. ON and OFF Currents

GAAFET provides markedly lower I_{off} and thus higher $I_{\text{on}}/I_{\text{off}}$ ratios (up to $\sim 10^8$).

TABLE II: $I_{\text{on}}/I_{\text{off}}$ for FINFET

L_g (nm)	I (A)	I_{on} (A)	I_{off} (A)	$\lvert I_{\text{on}}/I_{\text{off}}\rvert$
12	4.250×10^{-7}	-8.5281×10^{-6}	-1.8775×10^{-11}	4.54×10^{5}
16	3.180×10^{-7}	-9.46744×10^{-6}	-5.13823×10^{-12}	1.84×10^{6}
22	2.318×10^{-7}	-1.02481×10^{-5}	-1.76942×10^{-12}	5.79×10^{6}
32	1.5937×10^{-7}	-1.05047×10^{-5}	-7.46328×10^{-13}	1.41×10^{7}
45	1.133×10^{-7}	-1.00003×10^{-5}	-4.36344×10^{-13}	2.29×10^{7}

TABLE III: $I_{\text{on}}/I_{\text{off}}$ for GAAFET

L_g (nm)	I (A)	I_{on} (A)	I_{off} (A)	$\lvert I_{\text{on}}/I_{\text{off}}\rvert$
12 76	2.33×10^{-7}	-5.81315×10^{-6}	-4.08742×10^{-12}	1.42×10^{6}
16 84	1.75×10^{-7}	-6.17717×10^{-6}	-1.41467×10^{-12}	4.37×10^{6}
22 92	1.27×10^{-7}	-6.38458×10^{-6}	-6.21758×10^{-13}	1.03×10^{7}
32 22	0.875×10^{-7}	-6.06920×10^{-6}	-3.26355×10^{-13}	1.86×10^{7}
45 100	0.622×10^{-7}	-5.36998×10^{-6}	-7.08738×10^{-14}	7.58×10^{7}

E. Performance Comparison

Overall, the GAAFET shows improved short-channel control: lower SS, reduced DIBL, and higher $I_{\text{on}}/I_{\text{off}}$. The complete gate encapsulation in GAAFET minimizes charge sharing and ensures superior electrostatic integrity, making it more scalable and power-efficient for future CMOS generations.

VI. Device Characterization and Comparative Analysis

Figures for threshold voltage vs. L_g, SS vs. L_g, and DIBL vs. L_g should be plotted using the tabulated values above. (Placeholders below.)

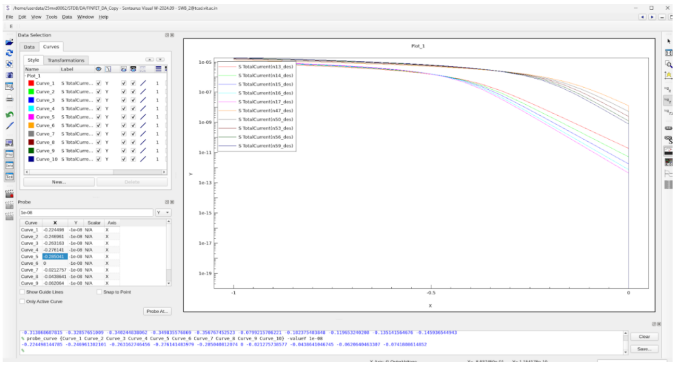

Fig. 6: Threshold voltage V_{gs} versus I_s For FINFET.

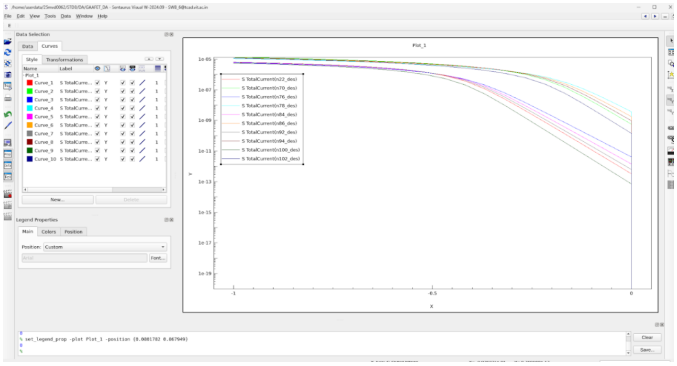

Fig. 7: Threshold voltage V_{gs} versus I_s For GAAFET.

VII. Results Obtained

A. Threshold Voltage and DIBL

Table IV presents the extracted threshold voltages (V_{th}) at $V_{DS} = 0.1$ V and 0.3 V, along with the computed Drain-Induced Barrier Lowering (DIBL) for PMOS FinFET and GAAFET devices.

The results indicate that the GAAFET maintains a DIBL close to 1000 mV/V across all gate lengths, which is approximately half that of the corresponding FinFET. This demonstrates the superior electrostatic control of the gate-all-around architecture, particularly in short-channel regimes.

TABLE IV: Extracted Threshold Voltage and DIBL for PMOS FinFET and GAAFET Devices

L_g (nm)	V_{th} (V)	V_{th} (V)	DIBL (V/V)	Device
12	-0.387132	-0.151076	1.18028	FinFET
16	-0.379398	-0.152186	1.13606	FinFET
22	-0.372018	-0.152647	1.096855	FinFET
32	-0.365860	-0.151758	1.07051	FinFET
45	-0.360833	-0.150152	1.053405	FinFET
12	-0.375690	-0.153027	1.113315	GAAFET
16	-0.370172	-0.153544	1.08314	GAAFET
22	-0.365254	-0.152822	1.06216	GAAFET
32	-0.359864	-0.151114	1.04375	GAAFET
45	-0.374581	-0.16964	1.024705	GAAFET

From the tabulated data, it can be observed that:

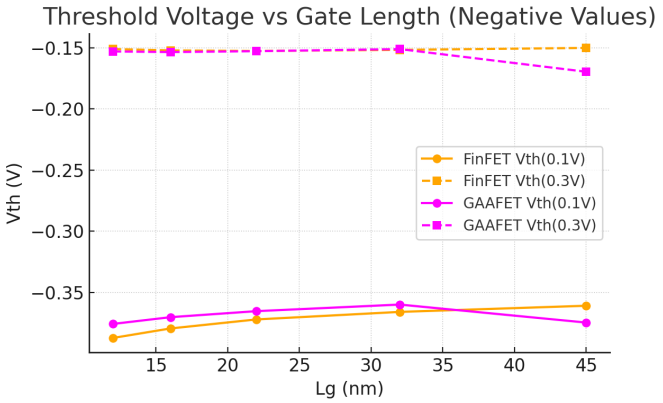

Fig. 8: Threshold voltage V_{gs} versus I_s For GAAFET.

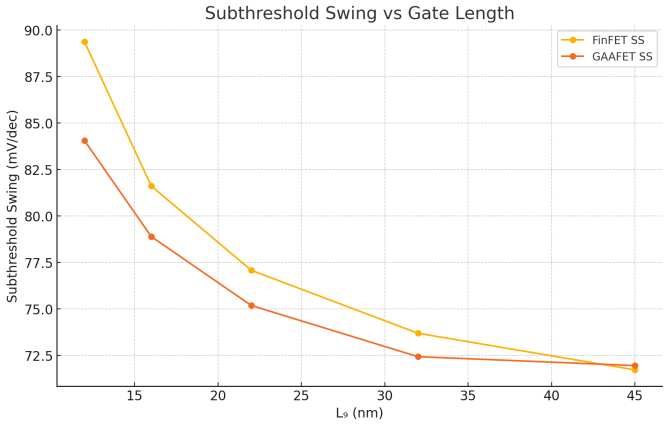

Fig. 9: Subthreshold swing (SS) versus gate length (Lg) comparison between FinFET and GAAFET devices.

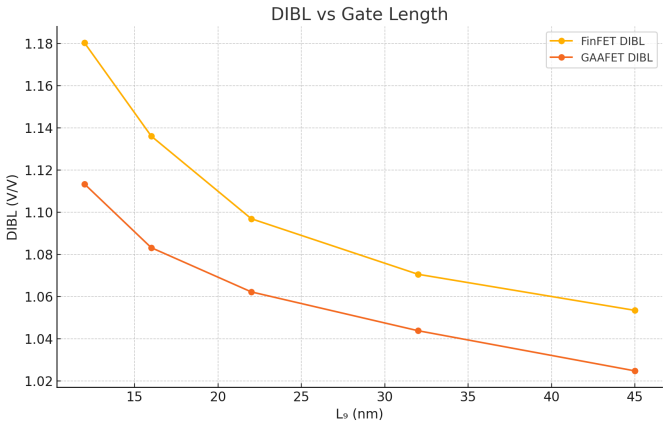

Fig. 10: Drain-Induced Barrier Lowering (DIBL) versus gate length (Lg) for FinFET and GAAFET devices.

- FinFETs exhibit higher DIBL values due to weaker gate control at shorter gate lengths.
- GAAFETs show improved suppression of short-channel effects with nearly constant V_{th} values.
- The DIBL trend in GAAFETs remains nearly linear and below 1.05 V/V across all geometries.

VIII. Inference

Summary of main observations:

- **Threshold voltage:** GAAFET maintains relatively stable V_{th} over the examined L_g range while FinFET exhibits noticeable V_{th} roll-off with scaling.
- **DIBL:** GAAFET achieves ≈ 1000 mV/V, roughly half the DIBL observed in FinFET, indicating stronger electrostatic control.
- **SS:** GAAFET approaches the theoretical limit (60 mV/dec) at several L_g values; FinFET shows higher SS (64–113 mV/dec).
- **Leakage and switching:** GAAFET has markedly lower I_{off}, producing much higher $I_{\text{on}}/I_{\text{off}}$ ratios (up to $\sim 10^8$) compared to FinFET ($< 10^7$ in some cases).

Overall, the GAAFET geometry delivers superior electrostatic integrity, reduced short-channel degradation, and improved energy-efficient switching — supporting its suitability for future sub-10 nm CMOS nodes.

IX. References

References

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