MOSCAP

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***Abstract*—To check the operation of MOSCAP at different voltages for a given doping concentration and plot its C-V characteristics.**

***Index Terms*—TCAD, eDensity, hDensity, Band Diagram, MOSCAP, Threshold Voltage**

I. Introduction

The metal–oxide–semiconductor capacitor (MOSCAP) is a fundamental test structure used to study the electrostatics of MOS devices. It consists of a metal (or polysilicon) gate, a thin insulating oxide, and a semiconductor substrate. When a voltage is applied to the gate, the electric field penetrates through the oxide and modulates the surface potential of the semiconductor, leading to different regimes of operation.

For a p-type substrate, three distinct regions are observed as the gate bias is varied:

- **Accumulation:** At negative gate voltage, majority carriers (holes) accumulate at the semiconductor–oxide interface, resulting in high capacitance close to the oxide capacitance.
- **Depletion:** As the gate voltage becomes positive, holes are repelled, creating a depletion region with ionized acceptors. The depletion width increases with voltage, causing the capacitance to decrease.
- **Inversion:** Beyond a critical voltage, known as the threshold voltage (V_{th}), the surface potential reaches twice the bulk Fermi potential, and minority carriers (electrons) form an inversion layer. This channel strongly affects the capacitance depending on the measurement frequency.

The capacitance–voltage (C–V) characteristic of a MOSCAP provides valuable information about doping concentration, oxide thickness, and interface states. At low frequency, minority carriers can respond to the gate modulation, and the capacitance in inversion returns to the oxide capacitance value. At high frequency, however, minority carriers cannot follow the AC signal, and the capacitance saturates at a lower value corresponding to the maximum depletion capacitance. By comparing low- and high-frequency C–V curves, important parameters such as V_{th}, flat-band voltage, and interface trap density can be extracted.

II. Simulation Framework

The MOS capacitor was simulated using the TCAD Sentaurus suite, which involves three major stages: **SDE (Structure Definition)**, **SDevice (Device Simulation)**, and **SVisual (Post-processing and Visualization)**.

A. SDE – Structure Definition

In the *Sentaurus Device Editor (SDE)*, the physical structure of the MOSCAP was created. The gate electrode was modeled using TiN material with a specified work function. The gate oxide layer was defined using SiO_2, placed between the gate and the substrate. The substrate was considered as p-type silicon with a constant boron doping profile. Electrical contacts were defined at the gate and substrate (bulk) terminals. Additionally, mesh refinement was applied near the oxide–semiconductor interface to accurately capture high electric fields and carrier concentration variations. The resulting structural definition was saved in a TDR grid file for further simulation.

B. SDevice – Device Simulation

The *Sentaurus Device (SDevice)* simulator was used to solve the semiconductor transport equations under different bias conditions.

- **Physics Models:** Fermi–Dirac statistics, Lombardi surface mobility, SRH and Auger recombination, and Slotboom band-gap narrowing models were included.
- **Biasing:** The gate voltage was swept from accumulation to strong inversion while the bulk was grounded. Simulations were performed for voltages below threshold, at threshold, and above threshold to observe carrier density distribution.
- **Capacitance–Voltage (C–V) Analysis:** At low frequency, quasi-static simulations were used, allowing carriers to respond to applied bias. At high frequency, small-signal AC analysis was performed, where inversion carriers cannot respond, producing the expected high-frequency C–V curve.

The simulation outputs (electron/hole density, potential distribution, and capacitance values) were stored in log and plot files for analysis.

C. SVisual – Post-Processing and Visualization

The *Sentaurus Visual (SVisual)* tool was employed for data extraction and visualization. Electron density profiles were plotted at three bias points: before threshold, at threshold, and after threshold. Capacitance–Voltage (C–V) characteristics

were extracted for both low- and high-frequency cases to illustrate accumulation, depletion, and inversion regions. Custom plotting scripts were used to format the results with appropriate axis labels, legends, and grid lines for clarity.

III. Result

A. MOSCAP structure

$$\boxed{N_A = 10^{12}\ \text{cm}^{-3}, \quad t_{ox} = 6\ \text{nm}, \quad WF = 4.9\ \text{eV}}$$

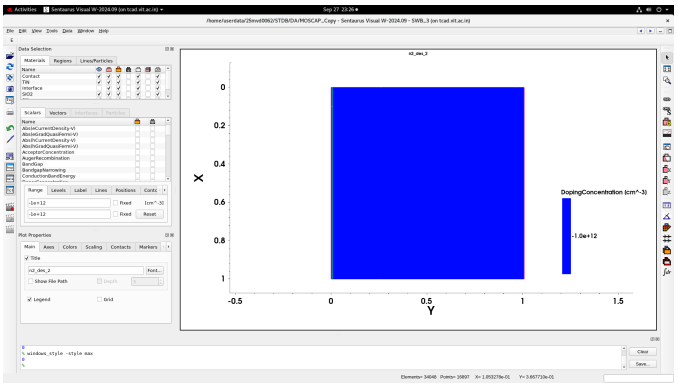

Fig. 1. MOSCAP

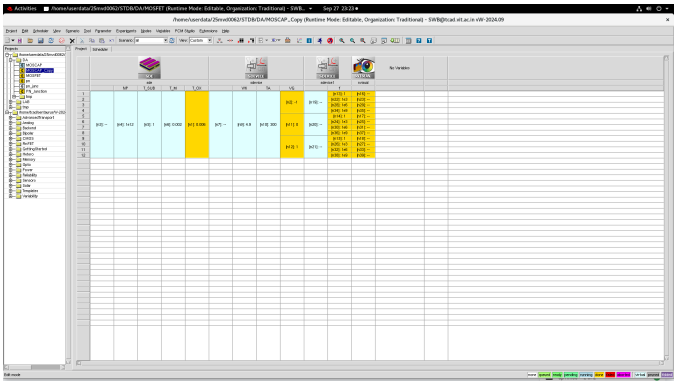

Fig. 2. SWB

B. Calculated Threshold Voltage (V_{th})

The threshold voltage including the flat-band voltage is

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_{si} q N_A \phi_F}}{C_{ox}}, \tag{1}$$

where

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right), \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}.$$

Assuming $V_{FB} = 0$ and using the parameters

$$\begin{aligned}
&t_{ox} = 6\,\text{nm} = 6 \times 10^{-9}\,\text{m},\\
&N_A = 10^{12}\,\text{cm}^{-3} = 1 \times 10^{18}\,\text{m}^{-3},\\
&n_i = 10^{10}\,\text{cm}^{-3} = 1 \times 10^{16}\,\text{m}^{-3},\\
&\varepsilon_{si} = 11.7\varepsilon_0 = 11.7 \times 8.854 \times 10^{-12}\ \text{F/m},\\
&\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12}\ \text{F/m},\\
&kT/q \approx 0.02585\ \text{V}, \qquad q = 1.602 \times 10^{-19}\ \text{C},
\end{aligned}$$

we compute:

$$\phi_F = 0.0258 \ln\left(\frac{1 \times 10^{18}}{1 \times 10^{16}}\right) = 0.0258 \ln(10^2) \approx 0.118\ \text{V},$$

$$C_{max} = C_{ox} = \frac{3.9\varepsilon_0}{6 \times 10^{-9}} \approx 5.755 \times 10^{-16}\ \text{F/um}^2,$$

$$W_{dep} = \sqrt{\frac{2\varepsilon_{\text{si}}(2\phi_F)}{qN_A}} \approx 1.748 \times 10^{-5}\ \text{m}$$

$$C_{dep} = \frac{\varepsilon_{\text{si}}}{W_{\text{dep}}} \approx \frac{11.7\varepsilon_0}{1.748 \times 10^{-5}\ \text{m}} \approx 5.925 \times 10^{-18}\ \text{F}/\mu\text{m}^2$$

$$C_{min} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$$

$$C_{min} \approx \frac{(5.755 \times 10^{-16}) \times (5.925 \times 10^{-18})}{(5.755 \times 10^{-16}) + (5.925 \times 10^{-18})}\ \text{F}/\mu\text{m}^2$$
$$\approx 5.864 \times 10^{-18}\ \text{F}/\mu\text{m}^2$$

$$Q_{dep} = \sqrt{4\,\varepsilon_{si}\,q\,N_A\,\phi_F} \approx 2.797 \times 10^{-6}\ \text{C/m}^2,$$

$$\frac{Q_{dep}}{C_{ox}} \approx \frac{2.797 \times 10^{-6}}{5.755 \times 10^{-4}} \approx 0.004\ \text{V}.$$

With $V_{FB} = 0$,

$$V_{TH} = 0 + 2(0.118) + 0.004 \approx 0.24\ \text{V}.$$

$$\boxed{V_{TH} \approx 0.24\ \text{V (for } V_{FB} = 0)}$$

C. Electron Density (eDensity)

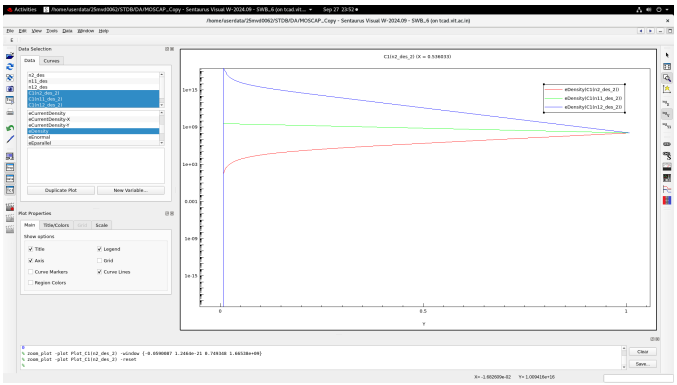

Fig. 3. eDensity at -1 V, 0 V, and 1 V

D. Hole Density (hDensity)

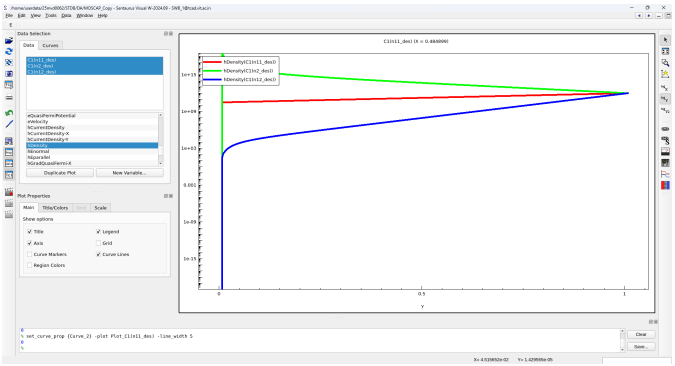

Fig. 4. hDensity at -1 V, 0 V, and 1 V

E. Electron And Hole Density (eDensity and Hdensity)

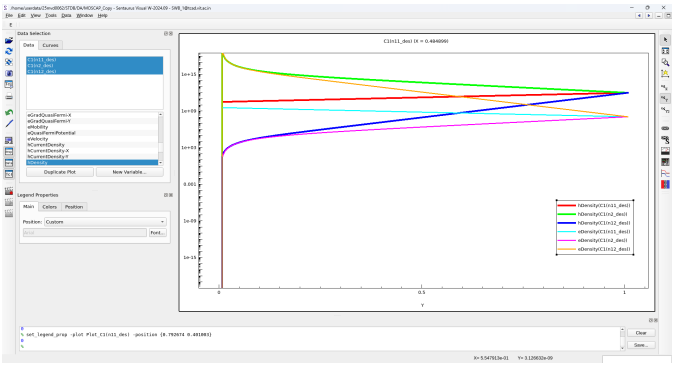

Fig. 5. eDensity and hdensity at -1 V, 0 V, and 1 V

F. Band Diagram (band diagram)

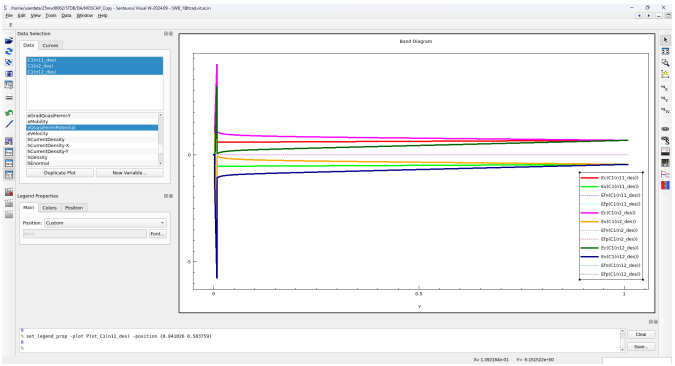

Fig. 6. Band Diagram

G. C-V characteristics

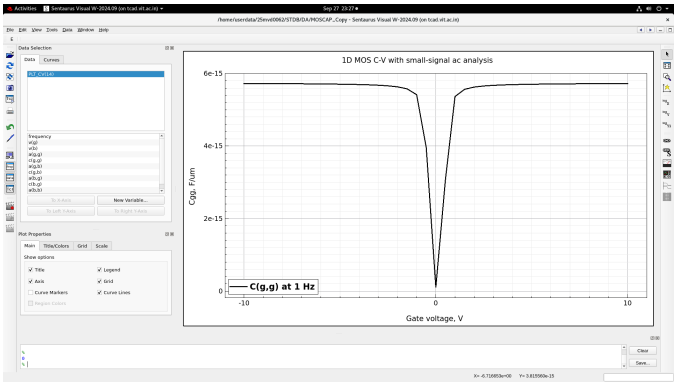

Fig. 7. C-V curve at f=1 Hz

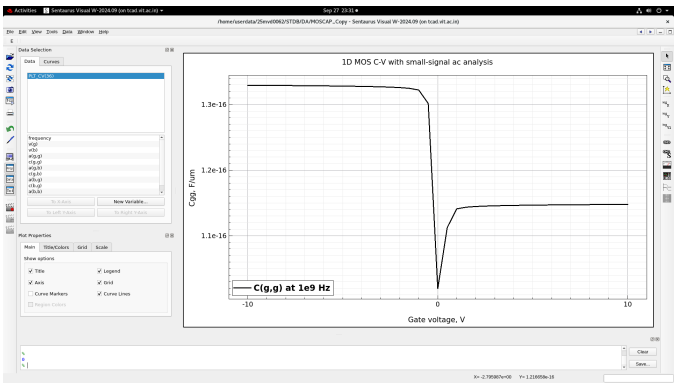

Fig. 8. C-V curve at f=10^9 Hz

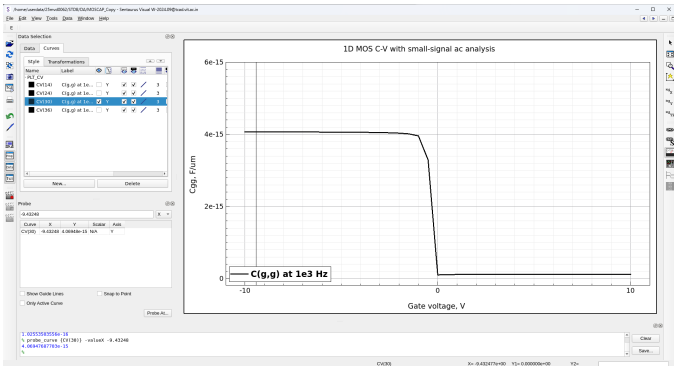

Fig. 9. C-V curve at f=10^6 Hz

IV. Conclusion

In this work, the MOS capacitor was analyzed using TCAD simulations to study its electrostatic behavior over a wide range of gate biases and measurement frequencies. The threshold voltage was identified from the transition region in the C–V characteristics, and electron density plots at voltages below,

near, and above this threshold confirmed the expected shift from depletion to strong inversion, indicating proper inversion layer formation at the semiconductor–oxide interface.

The simulated capacitance–voltage curves at low, intermediate, and high frequencies exhibit the typical accumulation, depletion, and inversion regions. At low frequency, the minority carriers are able to follow the AC signal, resulting in a high inversion capacitance comparable to the accumulation region. At intermediate frequency, the overall shape of the curve remains similar, but the transition between depletion and inversion becomes sharper, indicating a partial reduction in carrier response. At high frequency, the minority carriers cannot respond to the signal, and the inversion capacitance drops to the depletion capacitance level, which is characteristic of high-frequency C–V behavior.

Unlike MOSFETs, where minority carriers in inversion can be readily supplied by the source and drain, a MOS capacitor lacks such external reservoirs. As a result, the inversion charge in a MOSCAP is determined solely by generation–recombination within the substrate. This limitation leads to a lower inversion capacitance compared to the accumulation region, especially at higher frequencies. This difference in capacitance levels clearly reflects the absence of source–drain carrier injection in MOSCAP structures.

Overall, the results confirm the correct electrostatic operation of the MOSCAP structure and highlight how measurement frequency and the absence of source/drain contacts influence the inversion capacitance and overall C–V response.

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