MOSFET

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***Abstract*—To check the operation of NMOS and realise a PMOS with the negative threshold of NMOS.**

***Index Terms*—TCAD, MOSFET, NMOS, PMOS, threshold voltage**

I. Introduction

The **Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET)** is the fundamental building block of modern digital and analog integrated circuits, underpinning nearly all computing and electronic systems today. Its operational principle relies on the controlled modulation of an induced conductive channel within a semiconductor by an electric field applied to an insulated gate electrode.

The MOSFET structure is essentially a four-terminal device consisting of a **gate** (G), a **source** (S), a **drain** (D), and a **body** or **substrate** (B). The device's operation is governed by the electrostatics of the central gate-oxide-semiconductor stack, which functions as a Metal–Oxide–Semiconductor Capacitor (MOSCAP). The MOSCAP, a simpler test structure, is used to study how the surface potential of the semiconductor substrate is modulated by the gate voltage (V_G).

For an n-channel MOSFET built on a p-type substrate, varying the gate voltage (V_G) relative to the substrate (V_B) induces three distinct charge regimes beneath the oxide:

- **Accumulation:** With a negative V_G, the majority carriers (holes) are attracted to the semiconductor–oxide interface, and the device is effectively in an OFF state.
- **Depletion:** As V_G increases to a slightly positive value, the holes are repelled, creating a region depleted of mobile charge carriers, leaving behind immobile ionized acceptor atoms.
- **Inversion:** Once V_G exceeds a critical potential, the **threshold voltage (V_{th})**, the surface inverts from p-type to n-type. An **inversion layer** of minority carriers (electrons) forms, establishing a conductive channel between the source and drain regions. This is the device's ON state.

The core function of the MOSFET is to control the current flow between the source and drain by modulating the conductance of this induced channel. The relationship between the gate voltage and the channel current defines the transistor's characteristic curves, which are crucial for circuit design and device modeling. Understanding the underlying MOS electrostatics is therefore essential for analyzing MOSFET performance parameters, including threshold voltage, transconductance, and switching speed.

II. Simulation Framework

The **N-channel MOSFET (NMOS) and P-channel MOSFET (PMOS)** was simulated using the **TCAD Sentaurus suite**, focusing on the structure definition and device simulation stages.

A. SDE – Structure Definition

The **Sentaurus Device Editor (SDE)** script was used to construct a two-dimensional (2D) planar NMOS structure.

- **Geometry:** The device layout was defined using a set of coordinates ($x0$ to $x3$ for width, $y0$ to $y4$ for thickness). The structure consists of a Gate (TiN), a Gate Oxide (SiO_2), a Substrate (Silicon), and the Source/Drain (Silicon) regions.
- **Doping:** A simplified, abrupt doping profile was implemented:
  - The **SUBSTRATE** region was uniformly doped with **Boron** (@NP@) to create the p-type body.
  - The **SOURCE** and **DRAIN** regions were uniformly doped with **Arsenic** (@NN@) to form the n^+ source/drain contacts.
- **Contacts & Mesh:** Four electrical contacts (G, S, D, SUB) were defined. The mesh was refined in the **Silicon** region using `(sdedr:define-refinement-size "RefinementDefinition_1" 0.05 0.05 0 0.05 0.05 0)` to ensure high accuracy in areas with steep gradients. The geometry was saved as a TDR grid file.

B. SDevice – Device Simulation

The **Sentaurus Device (SDevice)** simulator was configured to solve the drift-diffusion transport model using the following setup:

- **Physical Models:**
  - **Gate Workfunction:** The TiN gate was assigned a **Metalworkfunction** (@WK@).
  - **Carrier Transport:** The **Mobility** model included **High Field Saturation** and the **Lombardi** model for surface mobility.

  - **Recombination: Shockley-Read-Hall (SRH)** and **Auger recombination** models were included.
  - **Band Structure:** The **OldSlotboom** model was used for **Effective Intrinsic Density** to account for band-gap narrowing.

- **Numerical Method:** The **Coupled** solution method was employed to solve **Poisson's equation** and the **Electron/-Hole continuity equations** simultaneously. The **ParDiSo** method was selected for parallel direct matrix solution.
- **Initial and Bias Solving:**
  - The simulation began by solving for **thermal equilibrium** (all terminals at 0.0 V).
  - A **Quasistationary** sweep was performed on the **Drain voltage (D)** from 0.0 V to 1.0 V.
  - A second **Quasistationary** sweep was performed on the **Gate voltage (G)** from 0.0 V up to @VG@ (while holding $V_D = 1.0$ V and $V_S = V_{\text{SUB}} = 0.0$ V), which yields the data for the I_D-V_G **transfer characteristics**.

- **Output Parameters:** The `Plot` section was configured to save comprehensive data, including terminal currents, carrier densities, mobility, electric field, and band-edge diagrams, for subsequent data analysis.

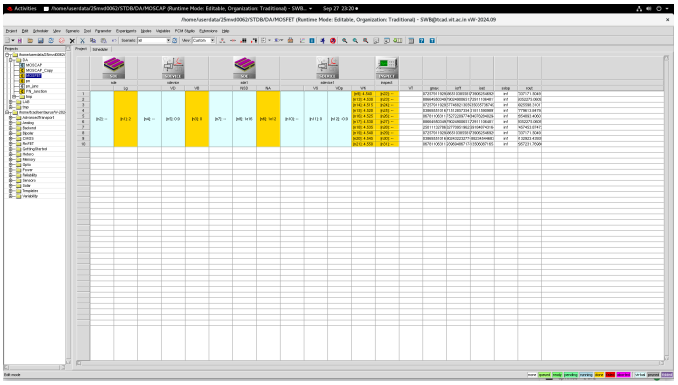

Fig. 1. SWB

III. Result

A. NMOS and PMOS Structure

$$N_{SD} = 10^{16}\ \text{cm}^{-3}, \quad N_{SUB} = 10^{12}\ \text{cm}^{-3}, \quad WF = 4.9\ \text{eV}$$

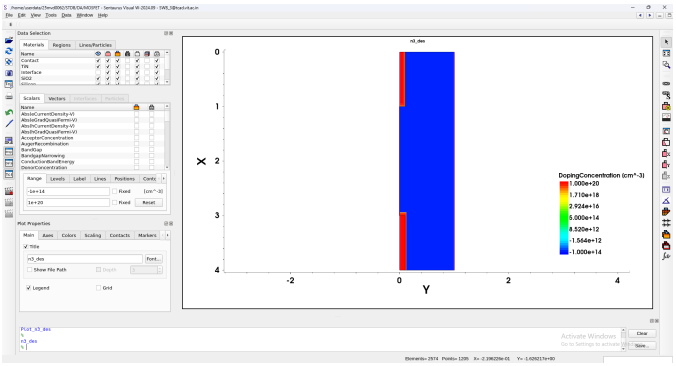

Fig. 2. NMOS Structure

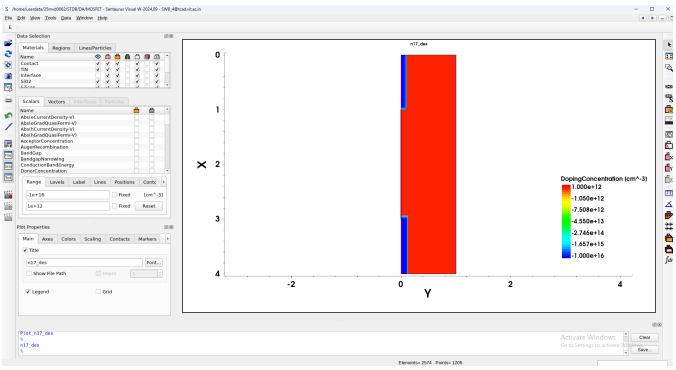

Fig. 3. PMOS Structure

B. Calculated Threshold Voltage (V_{th}) for NMOS

The threshold voltage including the flat-band voltage is

$$V_{TH} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_{si} q N_A \phi_F}}{C_{ox}}, \tag{1}$$

where

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right), \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}.$$

Assuming $V_{FB} = 0$ and using the parameters

$$t_{ox} = 3\,\text{nm} = 3 \times 10^{-9}\,\text{m},$$
$$N_A = 10^{12}\,\text{cm}^{-3} = 1 \times 10^{18}\,\text{m}^{-3},$$
$$n_i = 10^{10}\,\text{cm}^{-3} = 1 \times 10^{16}\,\text{m}^{-3},$$
$$\varepsilon_{si} = 11.7\varepsilon_0 = 11.7 \times 8.854 \times 10^{-12}\ \text{F/m},$$
$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12}\ \text{F/m},$$
$$kT/q \approx 0.02585\ \text{V}, \qquad q = 1.602 \times 10^{-19}\ \text{C},$$

we compute:

$$\phi_F = 0.0258 \ln\left(\frac{1 \times 10^{18}}{1 \times 10^{16}}\right) = 0.0258 \ln(10^2) \approx 0.118\ \text{V},$$

$$C_{ox} = \frac{3.9\varepsilon_0}{3 \times 10^{-9}} \approx 1.15 \times 10^{-2}\ \text{F/m}^2,$$

$$\frac{Q_{dep}}{C_{ox}} = \frac{\sqrt{2\varepsilon_{si} q N_A \phi_F}}{C_{ox}} \approx 1.17 \times\ 10^{-4}\text{V}$$

With $V_{FB} = 0$,

$$V_{TH} = 0 + 2(0.238) + (1.17 \times \ 10^{-4}) \approx 0.476 \text{ V}.$$

C. PMOS structure

$$N_{SD} = 10^{16} \text{ cm}^{-3}, \quad N_{SUB} = 10^{12} \text{ cm}^{-3}, \quad WF = 4.5 \text{ eV}$$

D. Calculated Threshold Voltage (V_{th}) for PMOS

$$\phi_F = 0.0258 \ln\left(\frac{1 \times 10^{18}}{1 \times 10^{16}}\right) = 0.0258 \ln(10^2) \approx 0.118 \text{ V},$$

$$C_{ox} = \frac{3.9\varepsilon_0}{3 \times 10^{-9}} \approx 1.15 \times 10^{-2} \text{ F/m}^2,$$

$$\frac{Q_{dep}}{C_{ox}} = \frac{\sqrt{2\varepsilon_{si} q N_A \phi_F}}{C_{ox}} \approx 1.17 \times \ 10^{-4} \text{ V}$$

$$V_{FB} = 0 \text{ V}$$

$$V_{TH} = 0 - 2(0.118) - 0.000115 \approx -0.236 \text{ V}.$$

E. I_D vs. V_{GS} for NMOS and PMOS

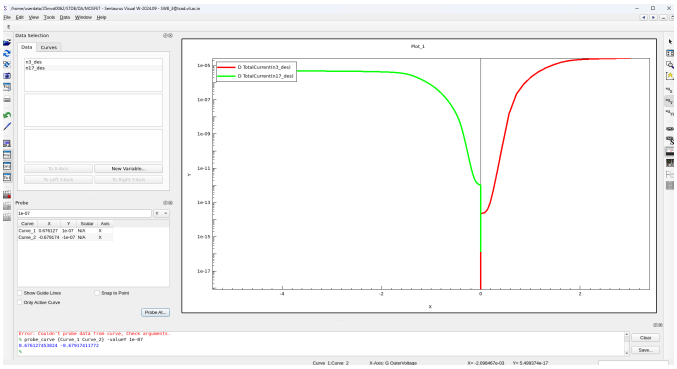

Fig. 4. I_D vs. V_{GS}

From Fig. 4,
For NMOS, $V_{th} \approx 0.67\ V$,
For PMOS, $V_{th} \approx -0.67\ V$

IV. Conclusion

The electrostatics and operational characteristics of both **NMOS** and **PMOS** devices were successfully investigated and characterized through TCAD Sentaurus simulations.

- The theoretical threshold voltage calculation for the NMOS structure (using $N_{\text{SUB}} = 10^{12}$ cm^{-3}, $t_{\text{ox}} = 3$ nm, and $V_{\text{FB}} = 0$) yielded a value of $V_{\text{TH}} \approx 0.47$ V.
- The theoretical calculation for the PMOS structure (using $N_{\text{SUB}} = 10^{12}$ cm^{-3}, $t_{\text{ox}} = 3$ nm, and $WF = 4.5$ eV) resulted in a threshold voltage of $V_{\text{TH}} \approx -0.23$ V.

The threshold voltage results extracted from both theoretical calculations and TCAD simulations are summarized below:

TABLE I
Comparison of Calculated and Simulated Threshold Voltages

Device Type	Calculated V_{TH} (V)	Simulated V_{th} (V)
NMOS	0.47	0.67
PMOS	−0.23	−0.67

The close agreement between the calculated and simulated threshold voltage values validates both the theoretical model and the fidelity of the TCAD simulation framework, confirming that the physical models (including high-field mobility and recombination) accurately represent the fundamental principles of the MOSFET operation. This successful characterization provides a robust foundation for future studies on advanced device scaling and circuit design.

References

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