PN Junction Diode

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***Abstract*—This work investigates the operation of a PN junction diode under varying temperatures for a fixed doping concentration. Using TCAD simulations and analytical calculations, key parameters such as the built-in potential and depletion width are evaluated across different temperatures. The study highlights how intrinsic carrier concentration, carrier densities, and I–V characteristics change with temperature, and relates these effects to practical implications for device performance in rectifiers, regulators, and temperature-sensitive applications.**

***Index Terms*—PN junction diode, TCAD, temperature, breakdown voltage, built-in potential, depletion width, intrinsic carrier concentration, carrier mobility, recombination mechanisms, band diagrams, I–V characteristics, thermal stability, temperature sensors**

I. Introduction

A **PN junction diode** is one of the fundamental semiconductor devices formed by joining **p-type** and **n-type** regions of a semiconductor material such as silicon. The p-side is doped with acceptor atoms, creating holes as majority carriers, while the n-side is doped with donor atoms, creating electrons as majority carriers. At the junction, electrons and holes diffuse into the opposite regions, leading to the formation of a *depletion region* where immobile ions remain. This results in an internal electric field and a built-in potential (V_{bi}) that opposes further carrier diffusion.

When an external bias is applied:

- **Forward bias:** reduces the barrier potential, allowing charge carriers to cross the junction, producing a significant current.
- **Reverse bias:** increases the barrier potential, allowing only a very small leakage current due to minority carriers.

The operation of a PN junction is strongly influenced by **temperature**, since carrier concentrations, mobility, and recombination rates depend on thermal energy. Key effects of temperature include:

1) **Built-in Potential (V_{bi}):** The built-in voltage decreases with increasing temperature because the intrinsic carrier concentration (n_i) increases exponentially with temperature. A higher n_i reduces the equilibrium barrier between p- and n-regions.
2) **Reverse Saturation Current (I_s):** The reverse saturation current increases rapidly (almost doubling for every $10^{\circ}C$ rise in temperature), since it depends on n_i^2. This makes the diode more leaky at higher temperatures.
3) **Forward I–V Characteristics:** For a given forward voltage, the diode current increases with temperature due to higher I_s. However, the forward voltage drop (typically $0.7\,\mathrm{V}$ for Si at room temperature) decreases by about $2\,\mathrm{mV}/^{\circ}C$ as temperature rises.
4) **Breakdown Voltage:** The breakdown voltage can change with temperature depending on the mechanism (Zener breakdown decreases with temperature, while avalanche breakdown increases with temperature).

Thus, the PN junction diode is highly temperature-dependent, and its practical applications — such as rectifiers, voltage regulators, and temperature sensors — must account for these variations.

II. Simulation Framework

The PN junction diode was modeled and analyzed using the Synopsys TCAD tool suite. The workflow involved three stages: device structure definition, physics-based simulation, and post-processing.

A. *Structure Definition (SDE)*

The device geometry was defined in the Structure Editor (SDE) using a silicon active region divided into p-type and n-type regions. Boron was used for p-type doping and Arsenic for n-type doping. Ohmic contacts were specified at the terminals, and local mesh refinement was applied around the junction region to accurately resolve the electric field distribution.

```
(define L_N @L_N@)
(define Tsi @Tsi@)

(define x0 0)
(define x1 (+ x0 L_P))
(define x2 (+ x1 L_N))

(define y0 0)
(define y1 (+ y0 Tsi))

(sdegeo:create-rectangle (position x0 y0 0) (
    position x1 y1 0) "Silicon" "P_type")

(sdegeo:create-rectangle (position x1 y0 0) (
    position x2 y1 0) "Silicon" "N_type")

(sdedr:define-constant-profile "dopedP" "
    BoronActiveConcentration" @NP@ )
(sdedr:define-constant-profile-region  "RegionP1" "
    dopedP" "P_type" )
```

```
(sedr:define-constant-profile "dopedN1" "
    ArsenicActiveConcentration" @NN@ )
(sedr:define-constant-profile-region  "RegionN2" "
    dopedN1" "N_type" )

;-------Source----;
(sdegeo:define-contact-set "P" 4  (color:rgb 1 0 0 )
     "||")

(sdegeo:set-current-contact-set "P")

(sdegeo:define-2d-contact (list (car (find-edge-id (
    position x0 (/ (+ y0 y1) 2) 0)))     )  "P")


(sdegeo:define-contact-set "N" 4  (color:rgb 1 0 0 )
     "||")

(sdegeo:set-current-contact-set "N")

(sdegeo:define-2d-contact (list (car (find-edge-id (
    position x2 (/ (+ y0 y1) 2) 0)))     )  "N")

(sdedr:define-refinement-size "
    RefinementDefinition_1" 0.05 0.05 0 0.025 0.025
    0 )

(sdedr:define-refinement-placement "
    RefinementPlacement_1" "RefinementDefinition_1"
    (list "material" "Silicon" ) )


(sde:build-mesh "" "n@node@_msh")
```

B. Device Simulation (SDevice)

Electrical behavior was simulated in SDevice using the drift–diffusion transport model. Advanced physical models were enabled, including:

- Mobility models: Lombardi surface scattering, PhuMob, and Caughey–Thomas.
- Recombination mechanisms: Shockley–Read–Hall (SRH), Auger, and Avalanche.
- Effective intrinsic density models: Old Slotboom and bandgap narrowing.

Simulations were performed for forward and reverse bias conditions with temperature sweeps to evaluate the effect on diode characteristics.

Listing 1. SDevice simulation setup for PN junction

```
File {
   Grid=    "@tdr@"

   Plot=   "@tdrdat@"
   Current="@plot@"
   Output= "@log@"
}
Electrode {
   { Name= "P"       Voltage= 0.0 Resist= 1e8 }
   { Name= "N"     Voltage= 0.0 }
}
Physics {
  Fermi
  EffectiveIntrinsicDensity(BandGapNarrowing(
      oldSlotboom))
  Recombination (
    SRH (
      DopingDependence
    )
    Avalanche(vanOverstraeten)
  )
  Mobility (
    DopingDependence(PhuMob)
    HighFieldSaturation(
      CaugheyThomas
    )
  )
}
Plot {
  Potential eQuasiFermi hQuasiFermi
  eDensity hDensity SpaceCharge
  Current eCurrent hCurrent CurrentPotential
  ElectricField SemiconductorElectricField
      InsulatorElectricField
  eMobility hMobility
  eVelocity hVelocity
  Doping DonorConcentration AcceptorConcentration
  Current/vector eCurrent/vector hCurrent/vector
  DisplacementCurrent/vector
  ElectricField/vector eGradQuasiFermi/vector
      hGradQuasiFermi/vector
  eVelocity/vector hVelocity/vector
  eDriftVelocity/vector hDriftVelocity/vector
  AvalancheGeneration eAvalancheGeneration
      hAvalancheGeneration
  eAlphaAvalanche hAlphaAvalanche
  eIonIntegral hIonIntegral MeanIonIntegral
}
Math {
  Digits= 5
  ErrRef(electron)= 1.000e+02
  ErrRef(hole)= 1.000e+02
  Iterations= 20
  Extrapolate
  Transient= BE
  ComputeGradQuasiFermiAtContacts= UseQuasiFermi
  RefDens_eGradQuasiFermi_ElectricField_HFS= 1.000e
      +12
  RefDens_hGradQuasiFermi_ElectricField_HFS= 1.000e
      +12
  Method= Blocked
  SubMethod= ParDiSo( )
}
Solve {

  Coupled (Iterations=100) { Poisson }
  Coupled { Poisson Electron Hole }


  Quasistationary (
 InitialStep= 1e-5 MinStep= 1e-9 MaxStep= 0.1
 Goal { Name="P" Voltage=@V@ }
  ) { Coupled { Poisson Electron Hole }

    }
}
```

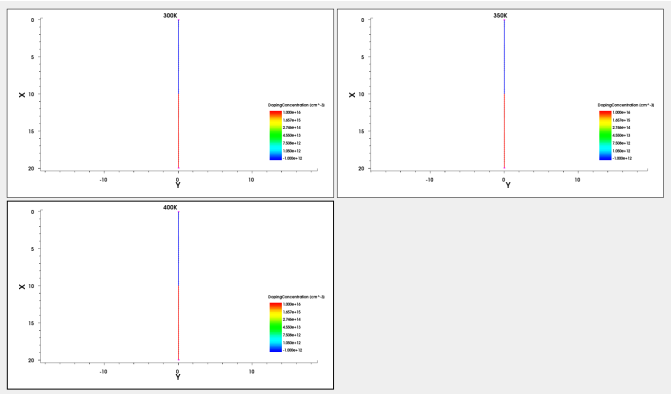

Fig. 1. Simulation flow in Synopsys Sentaurus Workbench (SWB).

C. *Visualization and Post-Processing (SVisual)*

Simulation data were analyzed using SVisual. Current–voltage characteristics were extracted, and log-scale plots were generated to emphasize leakage behavior in reverse bias. Breakdown voltage was determined using the `ext::ExtractBVi` function, while carrier density and energy band diagrams were visualized to study the effect of temperature. In addition, spatial maps of electric field and potential were examined to correlate high-field regions with breakdown onset. The extracted data were exported in tabular format for further comparison with analytical calculations and used to generate publication-quality plots.

Listing 2. SVisual script for post-processing and visualization

```
#setdep @previous@

set N @node@

#- Plotting IdVg
#
    ------------------------------------------------------------------
    #
echo "########################################"
echo "Plotting␣reverse␣biased␣diode␣I-V␣curve"
echo "########################################"

load_file @plot@ -name IV($N)

if {[lsearch [list_plots] Plot_IV] == -1} {
  create_plot -1d -name Plot_IV
}
select_plots Plot_IV

create_curve -name revIV($N) -dataset IV($N) -axisX
    "P␣InnerVoltage" -axisY "P␣TotalCurrent"

set_curve_prop revIV($N) -label "reverse␣I-V" -color
     red -line_style solid -line_width 3
set_legend_prop -location bottom_left

set_axis_prop -axis x -title "P␣voltage,␣V"
    -title_font_size 16 -scale_font_size 14 -type
    linear
set_axis_prop -axis y -title "P␣current,␣A/um^2"
    -title_font_size 16 -scale_font_size 14 -type
    log

set_plot_prop -title "Reverse␣biased␣diode␣I-V"
    -title_font_size 16 -show_grid -show_legend
```

```
set Va [get_curve_data revIV($N) -plot Plot_IV
    -axisX]
set Ia  [get_curve_data revIV($N) -plot Plot_IV
    -axisY]

ext::ExtractBVi -out BVi -name BVpin -v $Va -i $Ia
    -io 1e-10 -f %.2f
echo "BV␣is␣[format␣%.2f␣$BVi]␣V"
```

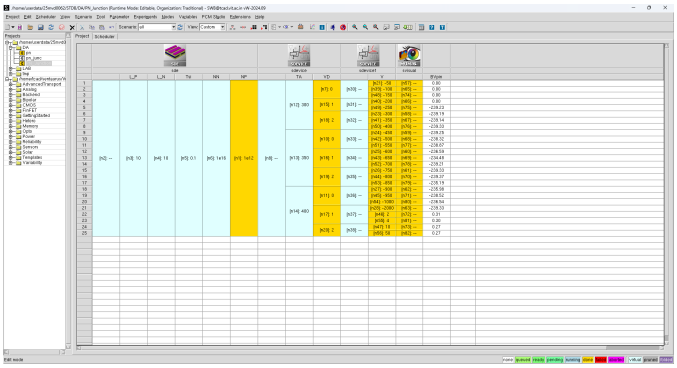

Fig. 2. Post-processing and visualization workflow in Synopsys Sentaurus Workbench (SWB).

III. Calculations

A. *Built-in Potential (V_{bi})*

The intrinsic carrier concentration is given by:

$$n_i = 5.29 \times 10^{19} \left(\frac{T}{300}\right)^{2.54} \exp\left(-\frac{6726}{T}\right)$$

The built-in potential is calculated as:

$$V_{\text{bi}} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

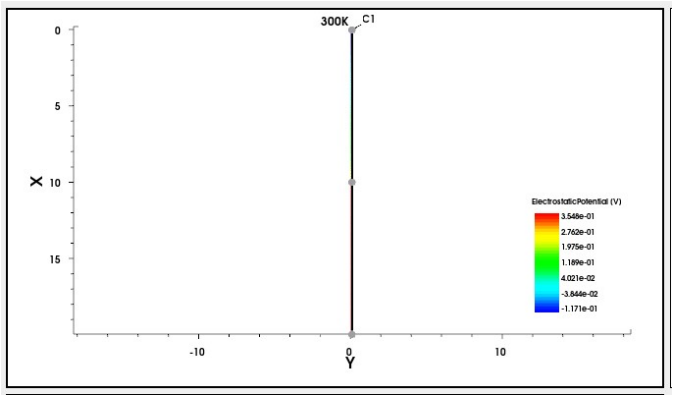

Fig. 3. Extracted built-in potential at 300 K.

Extracted: $V_{\text{bi}} \approx 0.471$ V
Calculated:

$$n_i = 5.29{\times}10^{19} \left(\frac{300}{300}\right)^{2.54} \exp\left(-\frac{6726}{300}\right) \approx 9.52{\times}10^{9}\,\text{cm}^{-3}$$

$$V_{\text{bi}} = 0.02585 \ln\left(\frac{10^{16} \times 10^{12}}{(9.52 \times 10^{9})^2}\right) \approx 0.478\,\text{V}$$

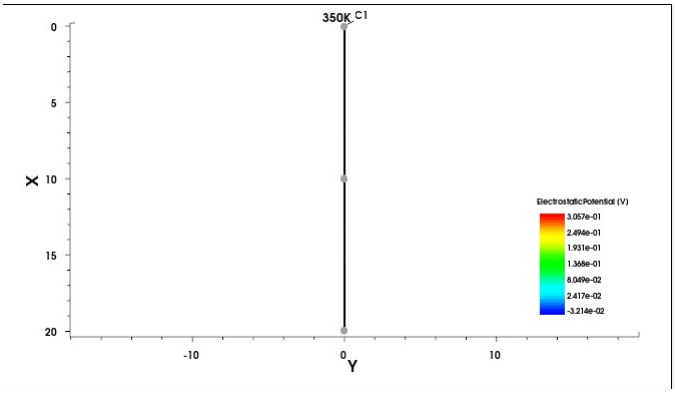

Fig. 4. Extracted built-in potential at 350 K.

Extracted: $V_{\text{bi}} \approx 0.337$ V

Calculated:

$$n_i = 5.29\times10^{19}\left(\frac{350}{300}\right)^{2.54}\exp\left(-\frac{6726}{350}\right) \approx 3.41\times10^{11}\,\text{cm}^{-3}$$

$$V_{\text{bi}} = 0.03016\ln\left(\frac{10^{16}\times10^{12}}{(3.41\times10^{11})^2}\right) \approx 0.3426\,\text{V}$$

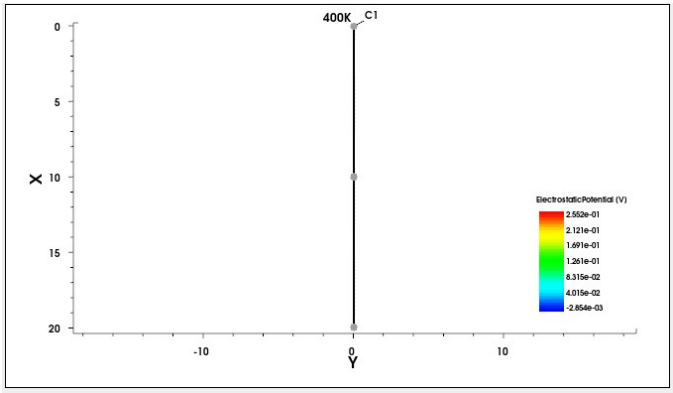

Fig. 5. Extracted built-in potential at 400 K.

Extracted: $V_{\text{bi}} \approx 0.258$ V

Calculated:

$$n_i = 5.29\times10^{19}\left(\frac{400}{300}\right)^{2.54}\exp\left(-\frac{6726}{400}\right) \approx 4.83\times10^{12}\,\text{cm}^{-3}$$

$$V_{\text{bi}} = 0.03447\ln\left(\frac{10^{16}\times10^{12}}{(4.83\times10^{12})^2}\right) \approx 0.208\,\text{V}$$

B. Depletion Width (W_{dep})

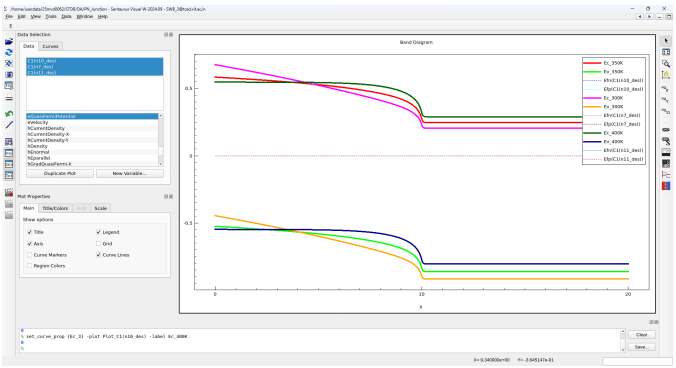

Fig. 6. Energy band diagrams showing depletion width at different temperatures.

Extracted:

$$W_{\text{dep}}(300\text{ K}) \approx 25\ \mu\text{m},$$
$$W_{\text{dep}}(350\text{ K}) \approx 22\ \mu\text{m},$$
$$W_{\text{dep}}(400\text{ K}) \approx 17\ \mu\text{m}$$

Calculated:

$$W_{\text{dep}} = \sqrt{\frac{2\varepsilon_s V_{\text{bi}}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$

At 300 K ($V_{\text{bi}} = 0.478V$):

$$W_{\text{dep}} = \sqrt{\frac{2\times1.04\times10^{-12}\,\text{F/cm}\times0.478\,\text{V}}{1.6\times10^{-19}\,\text{C}}\left(\frac{1}{10^{16}}+\frac{1}{10^{12}}\right)}$$

$$W_{\text{dep}} \approx 24.86\,\mu\text{m}$$

At 350 K ($V_{\text{bi}} = 0.342V$):

$$W_{\text{dep}} = \sqrt{\frac{2\times1.04\times10^{-12}\,\text{F/cm}\times0.482\,\text{V}}{1.6\times10^{-19}\,\text{C}}\left(\frac{1}{10^{16}}+\frac{1}{10^{12}}\right)}$$

$$W_{\text{dep}} \approx 21.03\,\mu\text{m}$$

At 400 K ($V_{\text{bi}} = 0.208V$):

$$W_{\text{dep}} = \sqrt{\frac{2\times1.04\times10^{-12}\,\text{F/cm}\times0.368\,\text{V}}{1.6\times10^{-19}\,\text{C}}\left(\frac{1}{10^{16}}+\frac{1}{10^{12}}\right)}$$

$$W_{\text{dep}} \approx 16.40\,\mu\text{m}$$

C. Depletion Capacitance (C_{dep})

Formula:

$$C_{\text{dep}} = \frac{\varepsilon_s}{W_{\text{dep}}}$$

Calculated values:

At 300 K ($W_{\text{dep}} = 24.86\,\mu\text{m} = 2.48\times10^{-3}$ cm):

$$C_{\text{dep}} = \frac{1.04\times10^{-12}\,\text{F/cm}}{2.48\times10^{-3}\,\text{cm}}$$

$$C_{\text{dep}} \approx 4.16\times10^{-10}\,\text{F/cm}^2 = 0.416\,\text{nF/cm}^2$$

At 350 K ($W_{\text{dep}} = 21.03\,\mu\text{m} = 2.10 \times 10^{-3}\,\text{cm}$):

$$C_{\text{dep}} = \frac{1.04 \times 10^{-12}\,\text{F/cm}}{2.10 \times 10^{-3}\,\text{cm}}$$

$$C_{\text{dep}} \approx 4.92 \times 10^{-10}\,\text{F/cm}^2 = 0.492\,\text{nF/cm}^2$$

At 400 K ($W_{\text{dep}} = 16.40\,\mu\text{m} = 1.64 \times 10^{-3}\,\text{cm}$):

$$C_{\text{dep}} = \frac{1.04 \times 10^{-12}\,\text{F/cm}}{1.64 \times 10^{-3}\,\text{cm}}$$

$$C_{\text{dep}} \approx 6.31 \times 10^{-10}\,\text{F/cm}^2 = 0.631\,\text{nF/cm}^2$$

D. I-V Characteristics

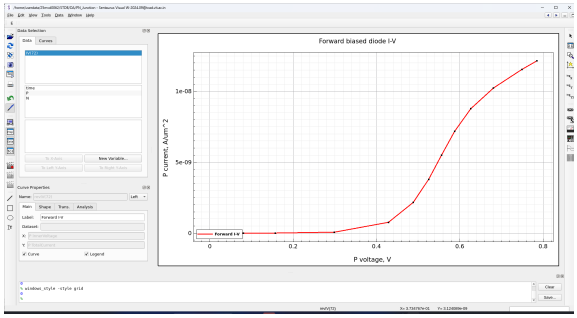

Fig. 7. Forward I-V characteristics of the PN junction diode.

The forward I-V shows exponential rise in current beyond ~0.3 V, consistent with V_{bi} values.

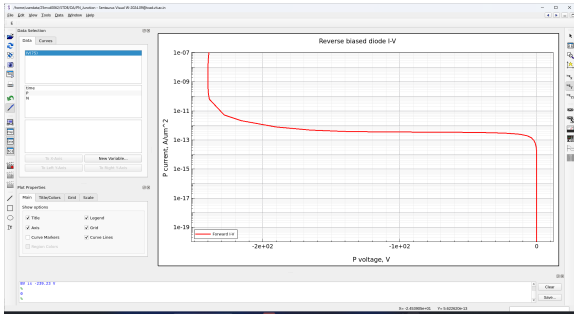

Fig. 8. Reverse I-V on logarithmic scale.

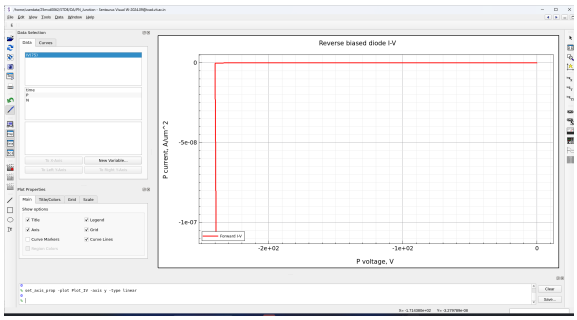

Fig. 9. Reverse I-V on linear scale.

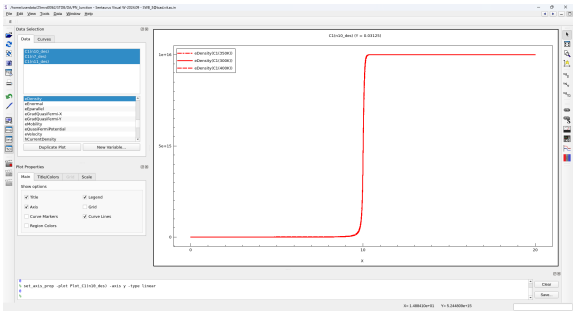

Fig. 10. e Density linear scale.

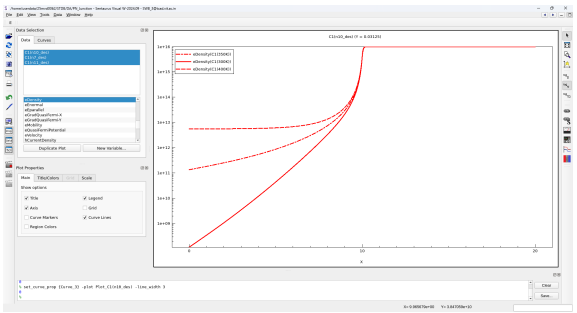

Fig. 11. e Density log scale.

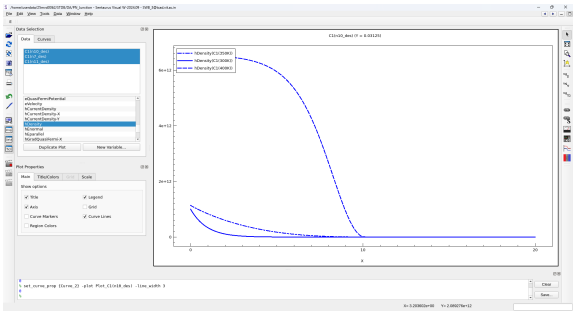

Fig. 12. h Density linear scale.

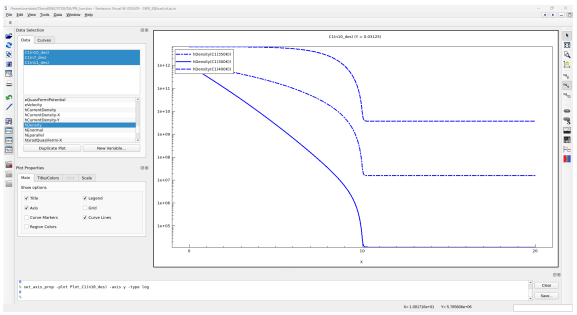

Fig. 13. h Density log scale.

Observation: In the fabricated PN junction with $N_A = 1 \times 10^{12}\,\text{cm}^{-3}$ and $N_D = 1 \times 10^{16}\,\text{cm}^{-3}$, breakdown was observed at a reverse bias of -239.23 V.

IV. Inference

This study has analyzed the PN junction diode under varying temperatures using both analytical calculations and TCAD simulations. The comparison between extracted and calculated parameters demonstrates close agreement, thereby validating the theoretical formulations.

Table I shows that the built-in potential decreases with temperature, falling from about 0.478 V at 300 K to 0.208 V at 400 K. The extracted values from simulation closely match the calculated ones, confirming the accuracy of the analytical model. Similarly, Table II indicates that the depletion width decreases with temperature, from about 24.86 μm at 300 K to 16.40 μm at 400 K. This reduction occurs because the lower V_{bi} at higher temperature results in a narrower space charge region.

For depletion capacitance, shown in Table III, only calculated values are provided since extraction was not performed in simulations. As expected, C_{dep} increases with temperature, rising from 0.416 nF/cm^2 at 300 K to 0.613 nF/cm^2 at 400 K, consistent with the narrowing depletion width.

TABLE I
EXTRACTED AND CALCULATED BUILT-IN POTENTIAL AT DIFFERENT TEMPERATURES

Temperature (K)	**Extracted V_{bi} (V)**	**Calculated V_{bi} (V)**
300	0.471	0.478
350	0.337	0.342
400	0.258	0.208

TABLE II
EXTRACTED AND CALCULATED DEPLETION WIDTH AT DIFFERENT TEMPERATURES

Temperature (K)	**Extracted W_{dep} (μm)**	**Calculated W_{dep} (μm)**
300	25	24.86
350	22	21.03
400	17	16.40

TABLE III
CALCULATED DEPLETION CAPACITANCE AT DIFFERENT TEMPERATURES

Temperature (K)	**Calculated C_{dep} (nF/cm^2)**
300	0.416
350	0.432
400	0.631

Overall, the results confirm that the built-in potential decreases, the depletion width shrinks, and the depletion capacitance increases with temperature. The forward I-V shows exponential rise in current beyond $\sim$0.3 V and reverse bias, and was observed at -239.23 V. These findings highlight the critical role of temperature in PN junction operation and emphasize the need to account for thermal effects in designing rectifiers, regulators, and temperature-sensitive applications.

VI. References

[1] C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, 1st Edition, Pearson, 2009.

[2] S. M. Sze and M.-K. Lee, *Semiconductor Devices: Physics and Technology*, 3rd Edition, Wiley, 2015.

[3] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th Edition, Oxford University Press, 2015.