Zailesh A R

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EDUCATION

M.Tech, VLSI Design	Vellore Institute of Technology, Vellore Campus	**8.42, 2027**
B.Tech, ECE	Govt. Model Engineering College, Thrikkakara, Kerala (KTU)	**8.06, 2023**
Class XII	Govt. Model Boys Higher Secondary School, Attingal, Kerala	**97.5%, 2018**
Class X	S.C.V.B.H.S, Chirayinkeezhu, Kerala	**10, 2016**

SKILLS & INTERESTS

Core Skills: Physical Design Flow, Physical Verification, Verilog HDL, TCL Scripting (Basics).
EDA Tools & OS: Cadence Virtuoso, VCS, Verdi, Design Compiler, PrimeTime, Formality, ICCII, Intel Quartus Prime, QuestaSim, DE2-115 (Cyclone IV) FPGA, Linux
Fields of Interest: Low Power IC Design, Digital IC Design, ASIC Design, TCL Scripting, Static Timing Analysis (STA)

WORK EXPERIENCE

Embedded Engineer, STEM CADETS Private Limited. *(1 year)*
Technologies: Proteus Design Suite, ESP boards.

- Designed and validated embedded circuits using ESP32/ESP8266 including sensor interfacing.
- Built and tested ESP-based IoT prototypes for product development.

PROJECTS

Design and Layout Implementation with Parasitic Extraction of 4-bit Array Multiplier **Individual Project**
Technologies: CMOS GPDK090, Cadence Virtuoso, Spectre, DRC/LVS

- Designed a 4-bit array multiplier using CMOS logic at transistor level with hierarchical gate-based construction.
- Constructed inverter, NAND and XOR gates to build full adders and a 4-bit ripple-carry adder architecture.
- Completed full-custom layout and attained DRC and LVS clean verification in GPDK090.
- Energy consumption was approximately **2 pJ** (average power $\approx$ **11.43 µW**).
- Final post-layout area was approximately $\mathbf{2086\ \mu m^2}$.

Timing-Constrained Implementation of Non-Restoring Square Root Algorithm **Team Size:** 3
Technologies: Verilog HDL, ModelSim, Intel Quartus Prime, DE2-115 FPGA, SDC

- Developed synthesizable Verilog RTL for a 4-bit non-restoring square root algorithm and verified all 16 input cases using ModelSim.
- Implemented the design on the DE2-115 FPGA with switch inputs and real-time output on 7-segment displays.
- Applied SDC constraints and achieved timing closure in Quartus with setup slack of **2.28 ns** and hold slack of **0.24 ns**.

RTL to GDS-II Implementation of High-Speed Multiplier (Ongoing) **Individual Project**
Technologies: Verilog HDL, Synopsys VCS, Design Compiler, Formality, PrimeTime

- Designed fully synthesizable Verilog RTL architecture and verified functional correctness using Synopsys VCS.
- Performed RTL-to-gate synthesis using Synopsys Design Compiler.
- Performed formal equivalence checking using Synopsys Formality to validate synthesis correctness.

Design and ASIC Implementation of RISC-V Processor with UART Peripheral (Ongoing) **Team Size:** 6
Technologies: Verilog HDL, Synopsys Design Compiler, Formality, PrimeTime, TCL, UART

- Developed modular RTL in Verilog for datapath, control unit, register file, ALU, and UART controller.
- Verified functional correctness using directed testbenches and waveform-based debugging.
- Performing RTL synthesis using Synopsys Design Compiler with custom TCL scripts.

Multi-feed Instant Home Automation IoT System **Team Size:** 4
Technologies: ESP8266, IoT, Blynk

- Built a multi-feed home automation system with bi-directional control.

COURSES & CERTIFICATIONS

- Programming with Python — Internshala (Certificate received)

POSITIONS OF RESPONSIBILITY

- **Chief Content Officer, IEDC MEC** – Managed a team of 24 members and coordinated a National-level Techno-Managerial event.
- **Content Manager, IEEE MEC SB** – Led a team of 20+ members and coordinated multiple events, including Overnight Hackathons.
- **Communications Coordinator, IETE MEC** – Handled official communications and coordinated various technical events.

ACTIVITIES & ACHIEVEMENTS

- Core Coordinator — MAGIC 2.0, conducted by IEEE MEC SB
- Core Coordinator — Technopreneur 2023, National Level event conducted by IEDC MEC.
- Delegate — Model United Nations MEC 2020
- Awards: Third prize (District), First prize (Sub-district) in Improvised Experiments Category, Kerala State Science Fair.